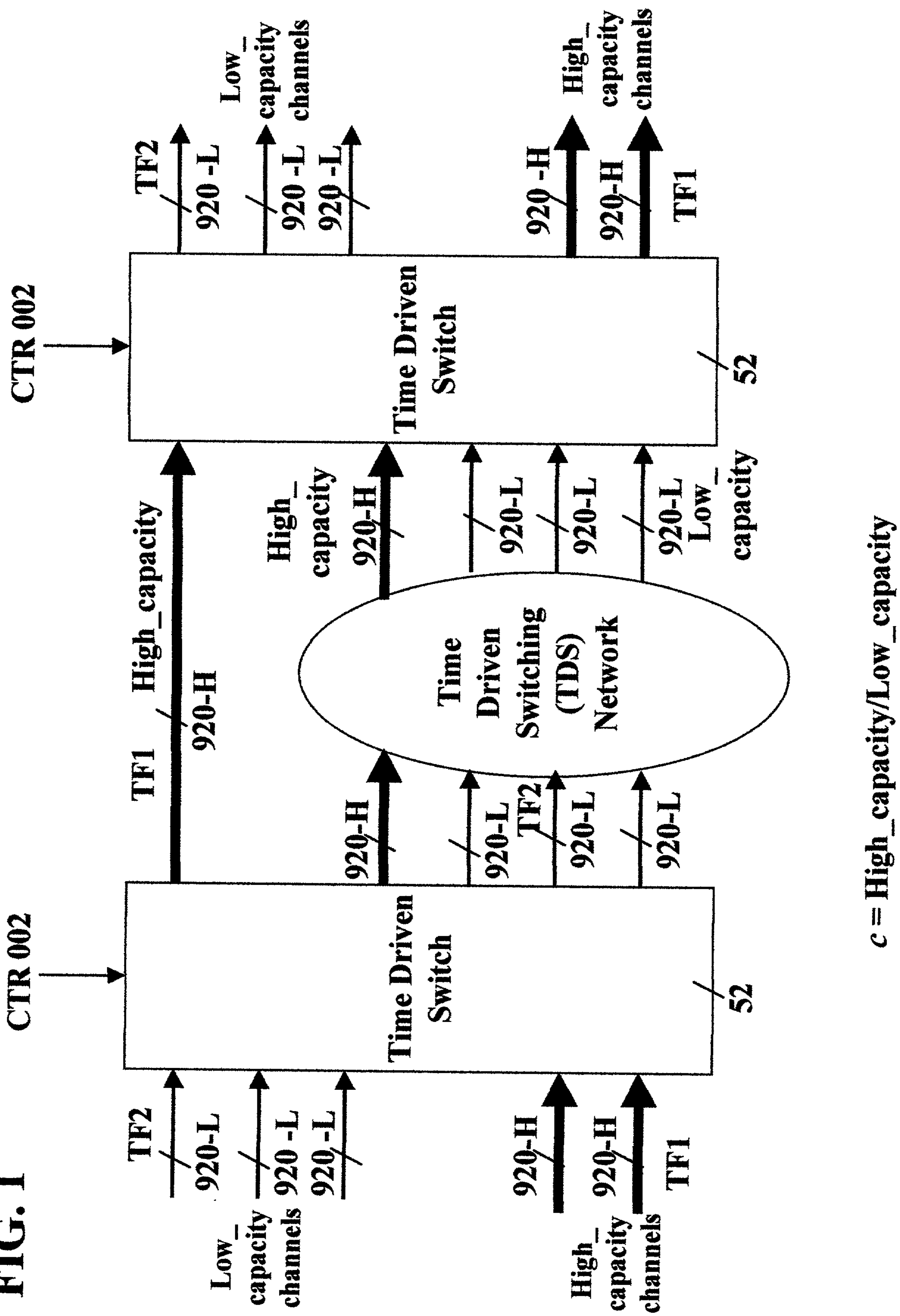
FIG. 1


CTR 002
Time Driven Switch
52
CTR 002
Time Driven Switch
52
Time Driven Switching (TDS) Network
Low_ capacity channels
High_ capacity channels
TF1
TF2
920-H
920-L
High_capacity
High_ capacity
Low_ capacity
c = High_capacity/Low_capacity

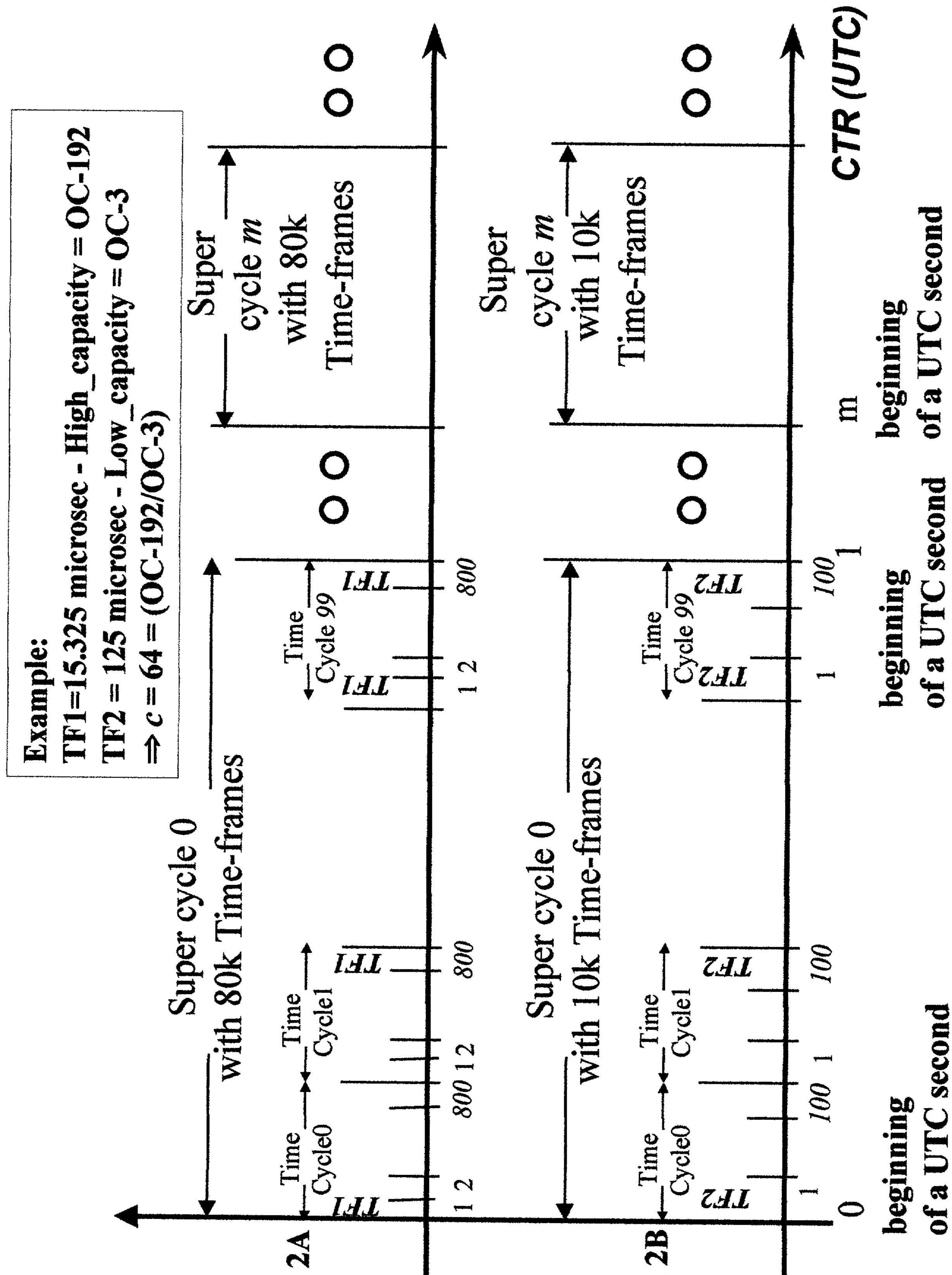

Example:
TF1=15.325 microsec - High_capacity = OC-192
TF2 = 125 microsec - Low_capacity = OC-3
⇒ c = 64 = (OC-192/OC-3)
Super cycle 0
With 80k Time-frames
Time Cycle0
Time Cycle1
TF1
1 2
800
800 1 2
Time Cycle 99
Super cycle m
with 80k
Time-frames
Super cycle 0
With 10k Time-frames
TF2
1
100
100 1
Super cycle m
with 10k
Time-frames
0
beginning
of a UTC second
1
m
CTR (UTC)

FIG. 2A

FIG. 2B

FIG. 3

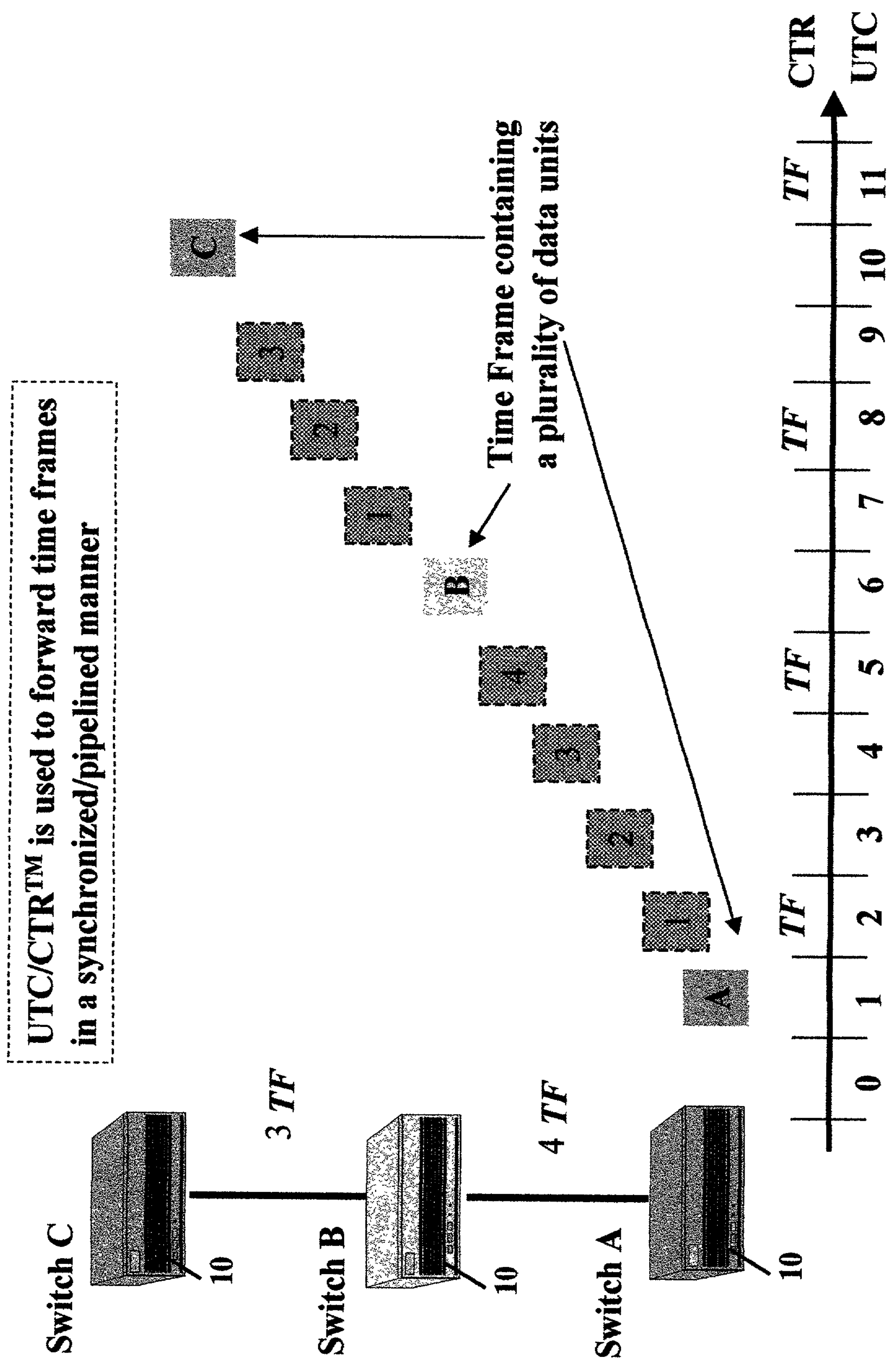

Switch C
Switch B
Switch A
10
10
10
3 TF
4 TF
UTC/CTR™ is used to forward time frames in a synchronized/pipelined manner
Time Frame containing a plurality of data units
A
1
2
3
4
B
1
2
3
C
TF
TF
TF
TF
0
1
2
3
4
5
6
7
8
9
10
11
CTR
UTC

FIG. 4A

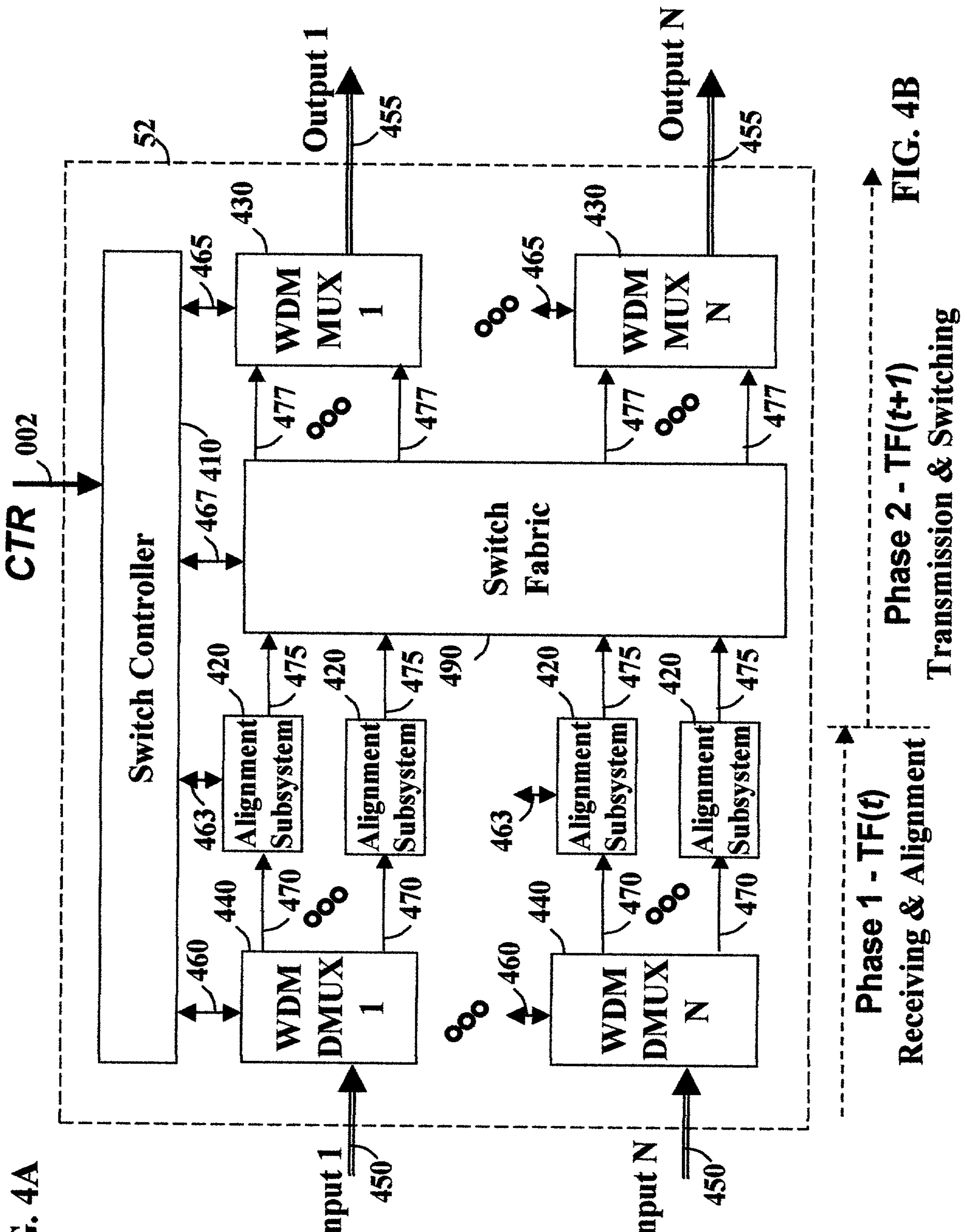

CTR
002
52
Switch Controller
Input 1
450
Input N
450
WDM DMUX 1
WDM DMUX N
460
440
470
463
Alignment Subsystem
420
475
490
467
410
Switch Fabric
477
465
WDM MUX 1
WDM MUX N
430
455
Output 1
Output N
Phase 1 - TF(t)
Receiving & Alignment
Phase 2 - TF(t+1)
Transmission & Switching

FIG. 4B

FIG. 5

Two time intervals: SC1_length·TF1 = 1 UTC second

- SC2_length·TF2 = 1 UTC second
- TF2 = (SC1_length / SC2_length) · TF1 = k · TF1, where the time cycles of TF1 and TF2 are aligned with respect to UTC.

For $\boldsymbol{k}$ = 2 and $\boldsymbol{c}$ = 4 (e.g., High_capacity=OC-192, Low_capacity=OC-48):

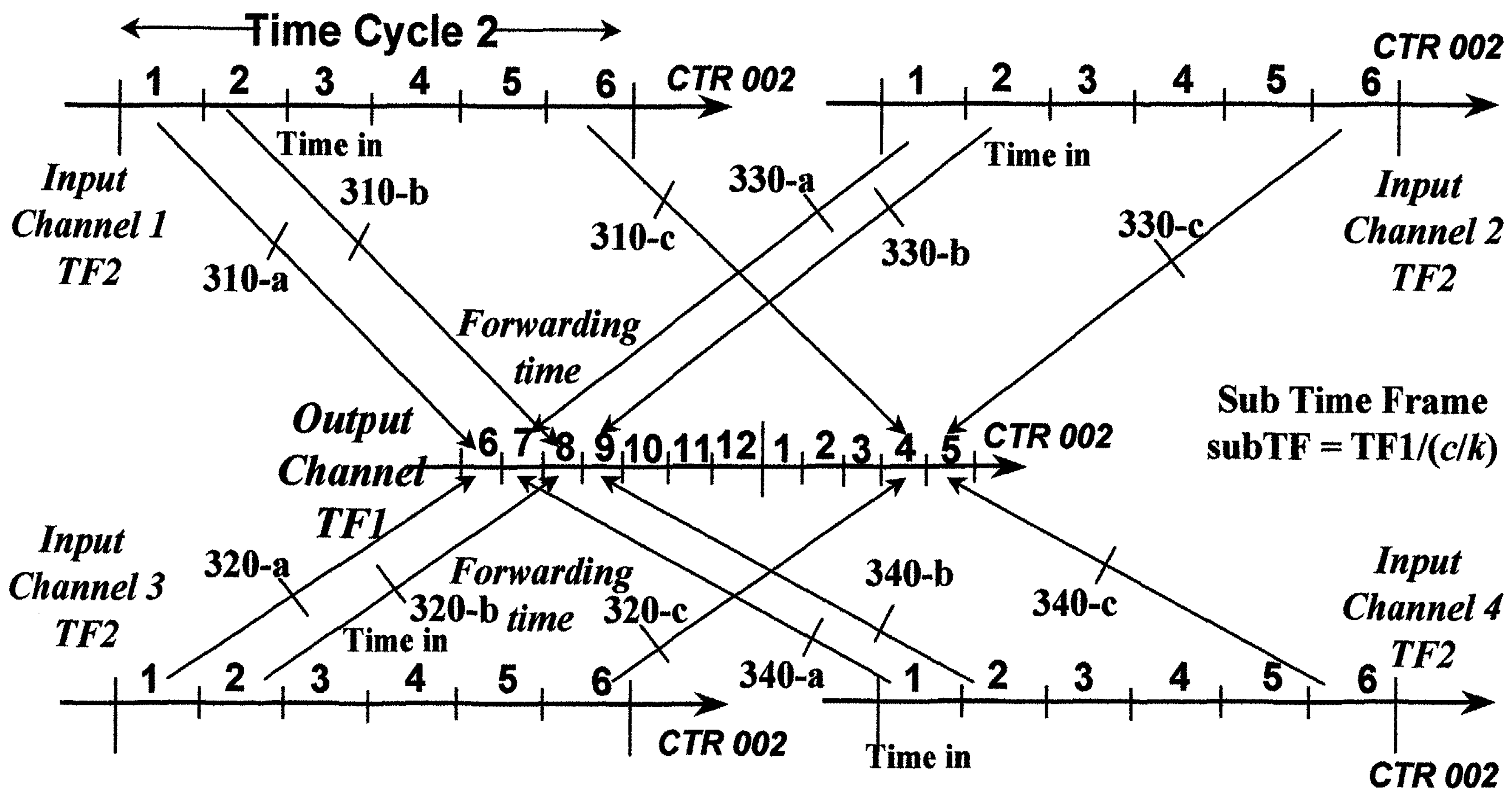


FIG. 6 Two time intervals: $SC1\_length \cdot TF1 = 1$ **UTC second**

- $SC2\_length \cdot TF2 = 1$ **UTC second**
- $TF2 = (SC1\_length / SC2\_length) \cdot TF1 = k \cdot TF1$, where the time cycles of ***TF1*** and ***TF2*** are aligned with respect to UTC.

For $k = 2$ and $c = 4$ (e.g., High_capacity=OC-192, Low_capacity=OC-48):

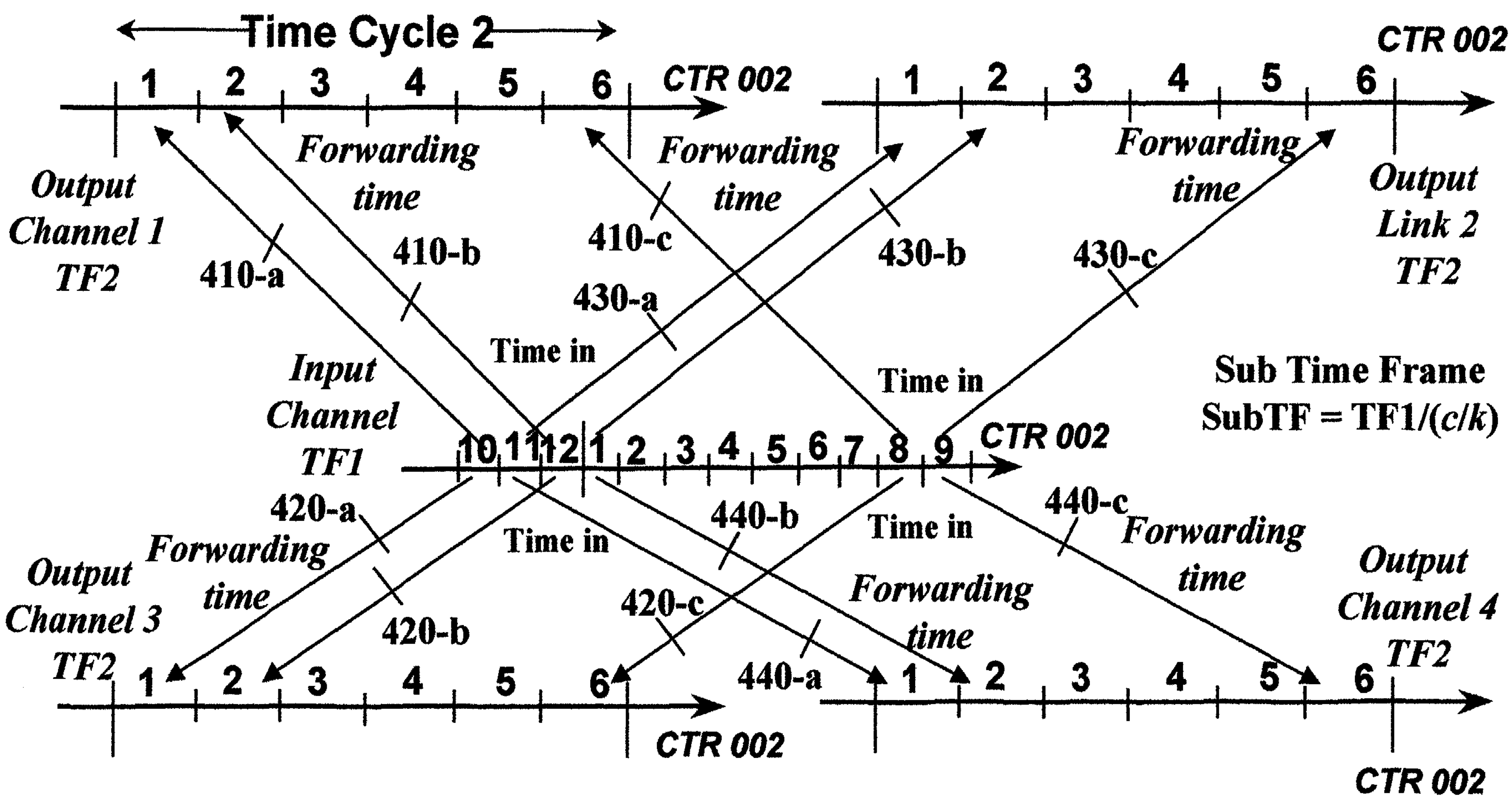


FIG. 7 Two time intervals: $SC1\_length \cdot TF1 = 1$ UTC second

- $SC2\_length \cdot TF2 = 1$ UTC second
- $TF2 = (SC1\_length / SC2\_length) \cdot TF1 = k \cdot TF1$, where the time cycles of $TF1$ and $TF2$ are aligned with respect to UTC.

For $k = 2$ and $c = 4$ (e.g., High_capacity=OC-192, Low_capacity=OC-48):

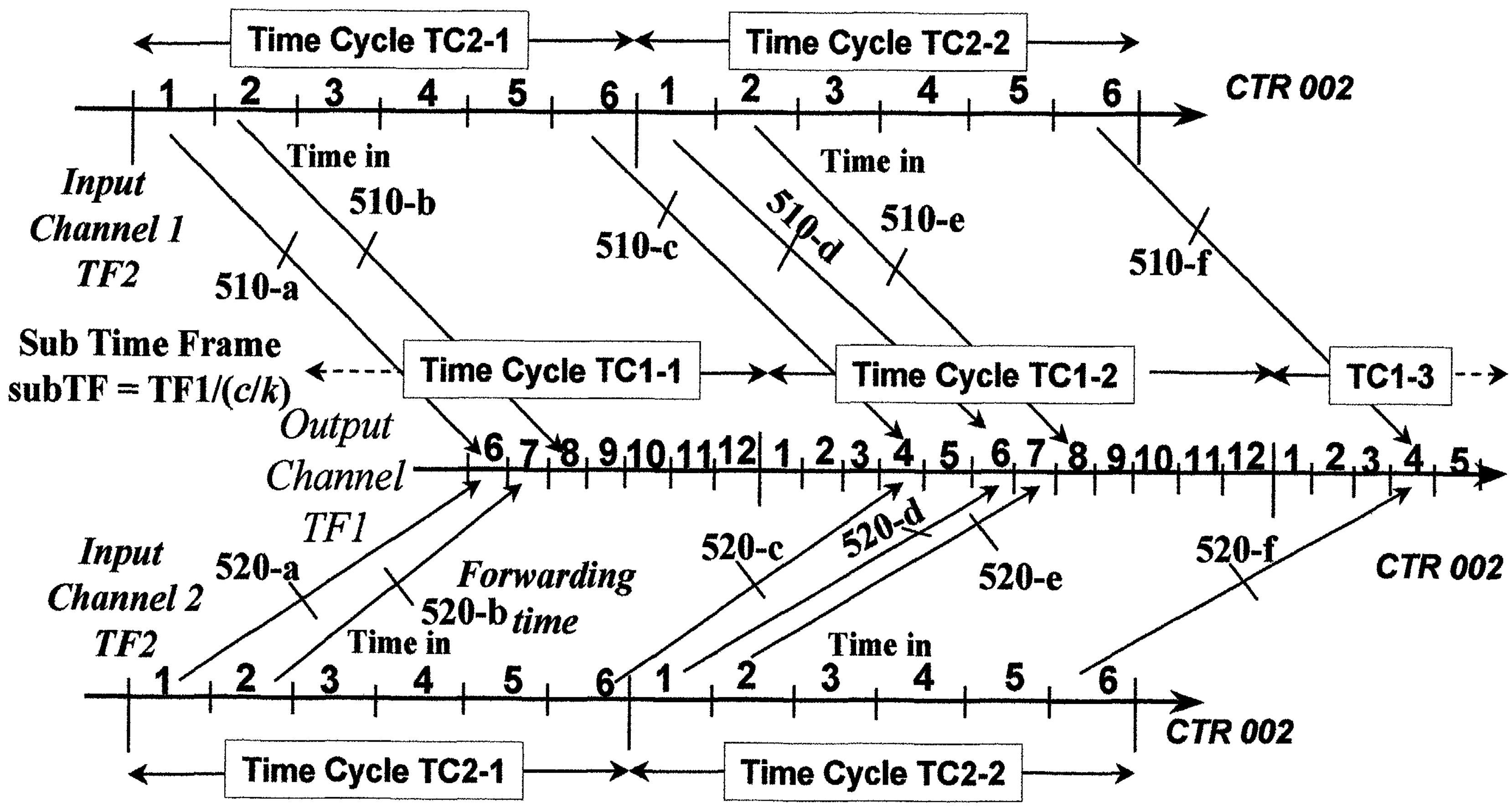


FIG. 8

Two time intervals: $SC1\_length \cdot TF1 = 1$ UTC second

- $SC2\_length \cdot TF2 = 1$ UTC second
- $TF2 = (SC1\_length / SC2\_length) \cdot TF1 = k \cdot TF1$, where the time cycles of $TF1$ and $TF2$ are aligned with respect to UTC.

For $k = 2$ and $c = 4$ (e.g., High_capacity=OC-192, Low_capacity=OC-48):

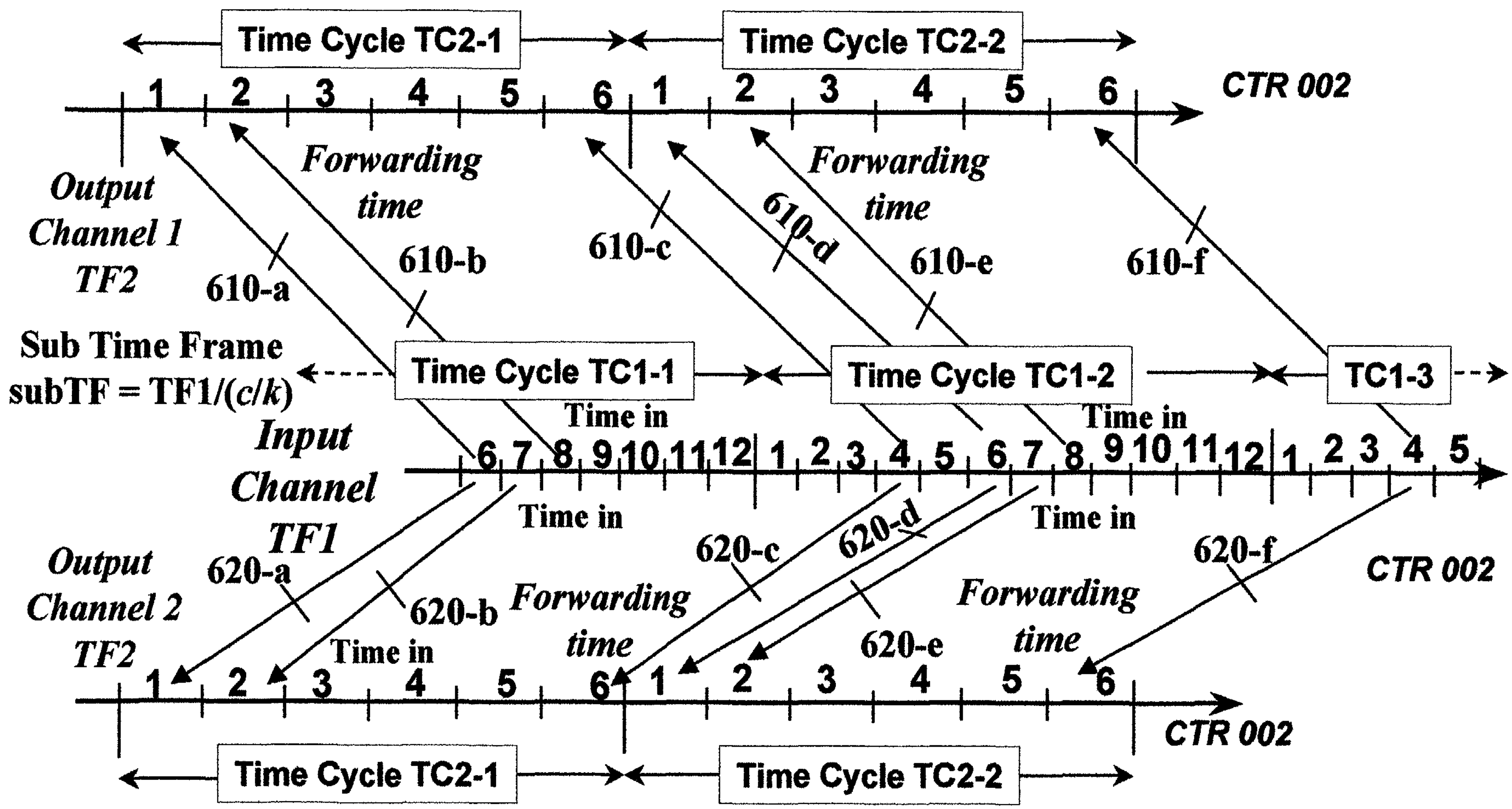


FIG. 9

c=4, e.g., OC-192/OC-48
k=2, e.g., 25 microsec/12.5 microsec

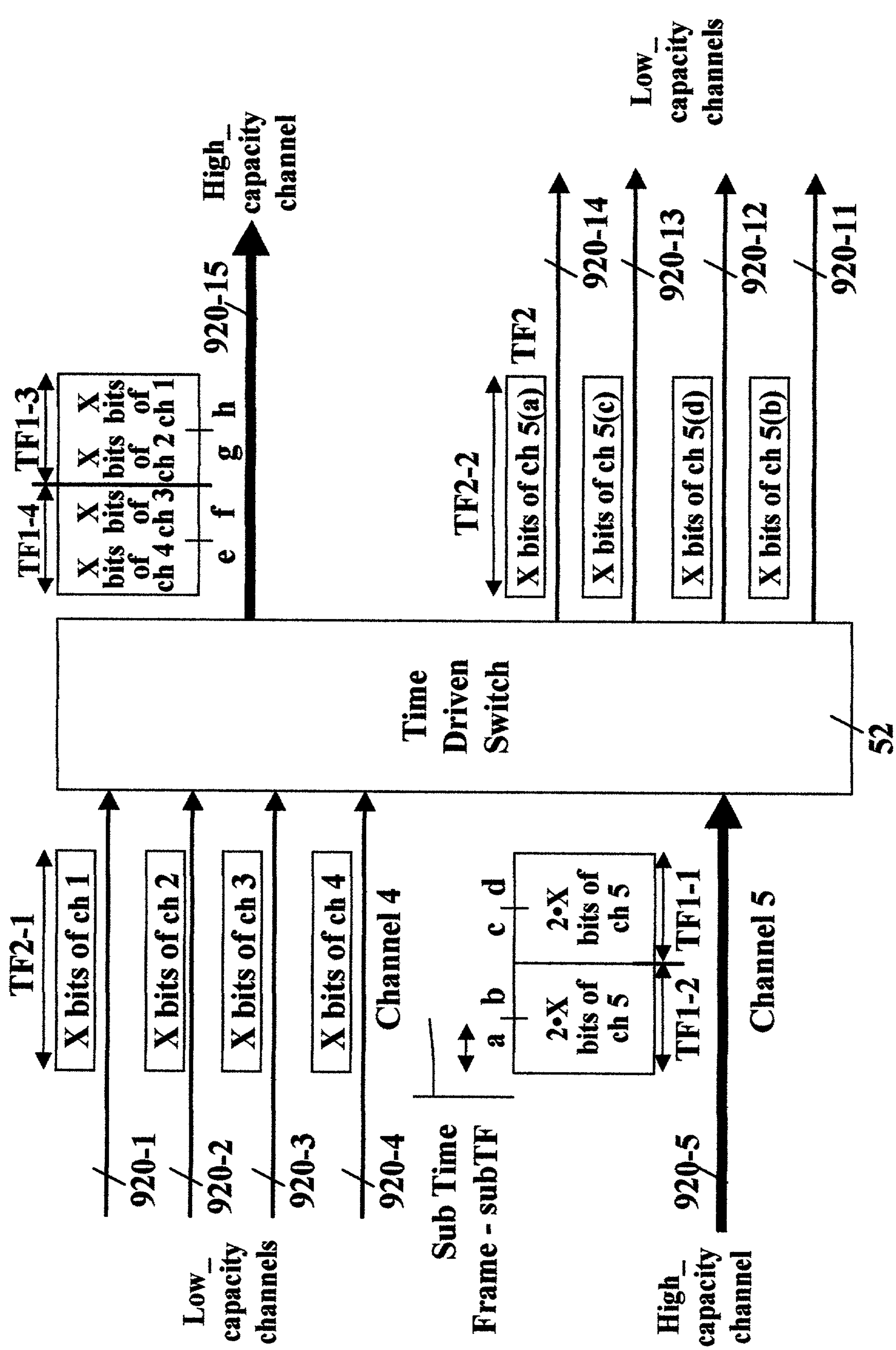


FIG. 10

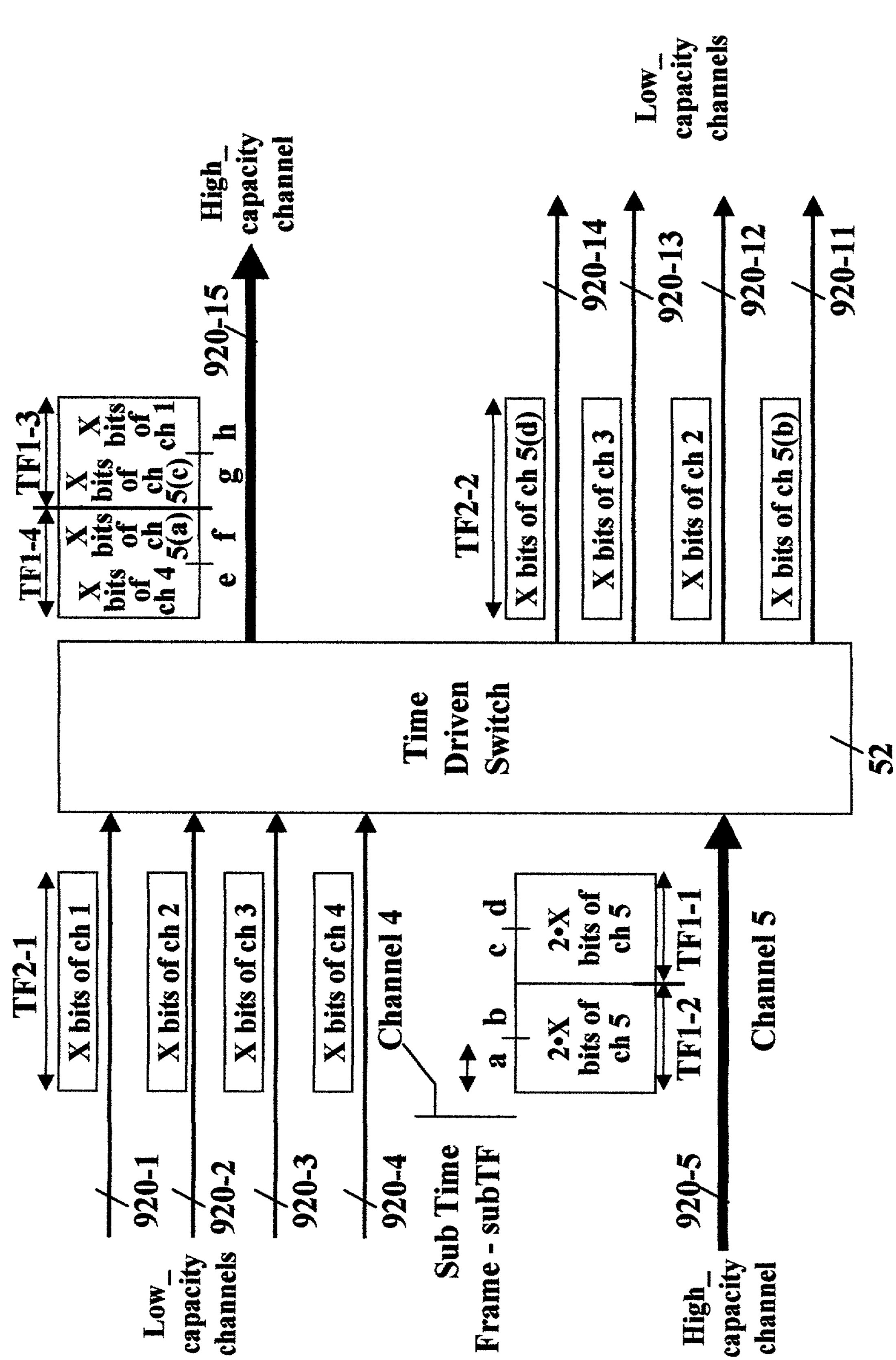

c=4, e.g., OC-192/OC-48
k=2, e.g., 25 microsec/12.5 microsec
Low_ capacity channels
920-1
920-2
920-3
920-4
TF2-1
X bits of ch 1
X bits of ch 2
X bits of ch 3
X bits of ch 4
Channel 4
Sub Time Frame - subTF
a
b
c
d
2•X bits of ch 5
2•X bits of ch 5
TF1-2
TF1-1
Channel 5
920-5
High_ capacity channel
Time Driven Switch
52
TF1-4
TF1-3
X bits of ch 4
X bits of ch 5(a)
X bits of ch 5(c)
X bits of ch 1
e
f
g
h
920-15
High_ capacity channel
TF2-2
X bits of ch 5(d)
X bits of ch 3
X bits of ch 2
X bits of ch 5(b)
920-14
920-13
920-12
920-11
Low_ capacity channels

FIG. 11

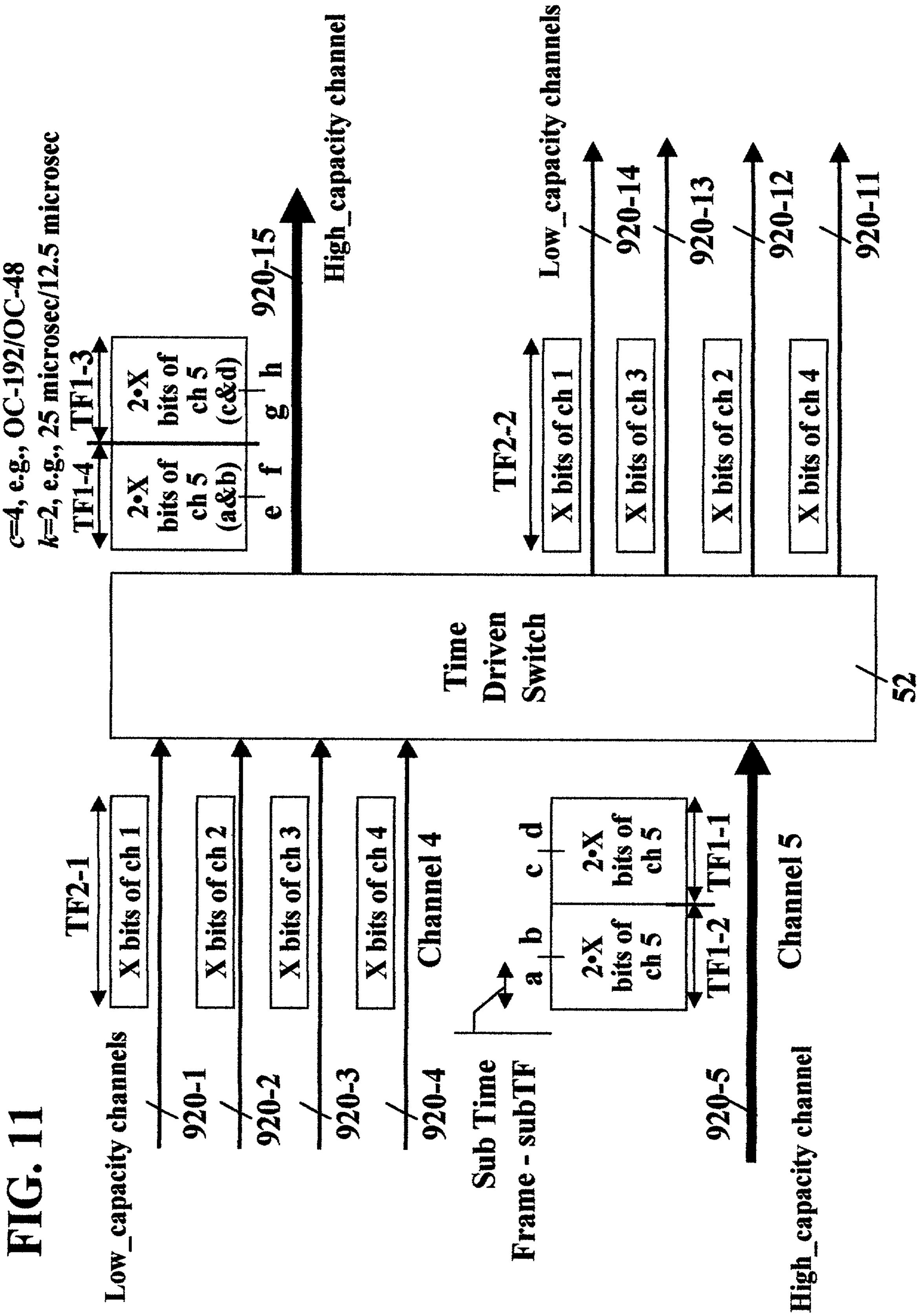

c=4, e.g., OC-192/OC-48
k=2, e.g., 25 microsec/12.5 microsec
Low_capacity channels
920-1
920-2
920-3
920-4
TF2-1
X bits of ch 1
X bits of ch 2
X bits of ch 3
X bits of ch 4
Channel 4
Sub Time
Frame - subTF
a b c d
2•X bits of ch 5
2•X bits of ch 5
TF1-2
TF1-1
Channel 5
920-5
High_capacity channel
Time
Driven
Switch
52
TF1-4
TF1-3
2•X bits of ch 5 (a&b)
2•X bits of ch 5 (c&d)
e f g h
920-15
High_capacity channel
TF2-2
X bits of ch 1
X bits of ch 3
X bits of ch 2
X bits of ch 4
Low_capacity channels
920-14
920-13
920-12
920-11

FIG. 12A

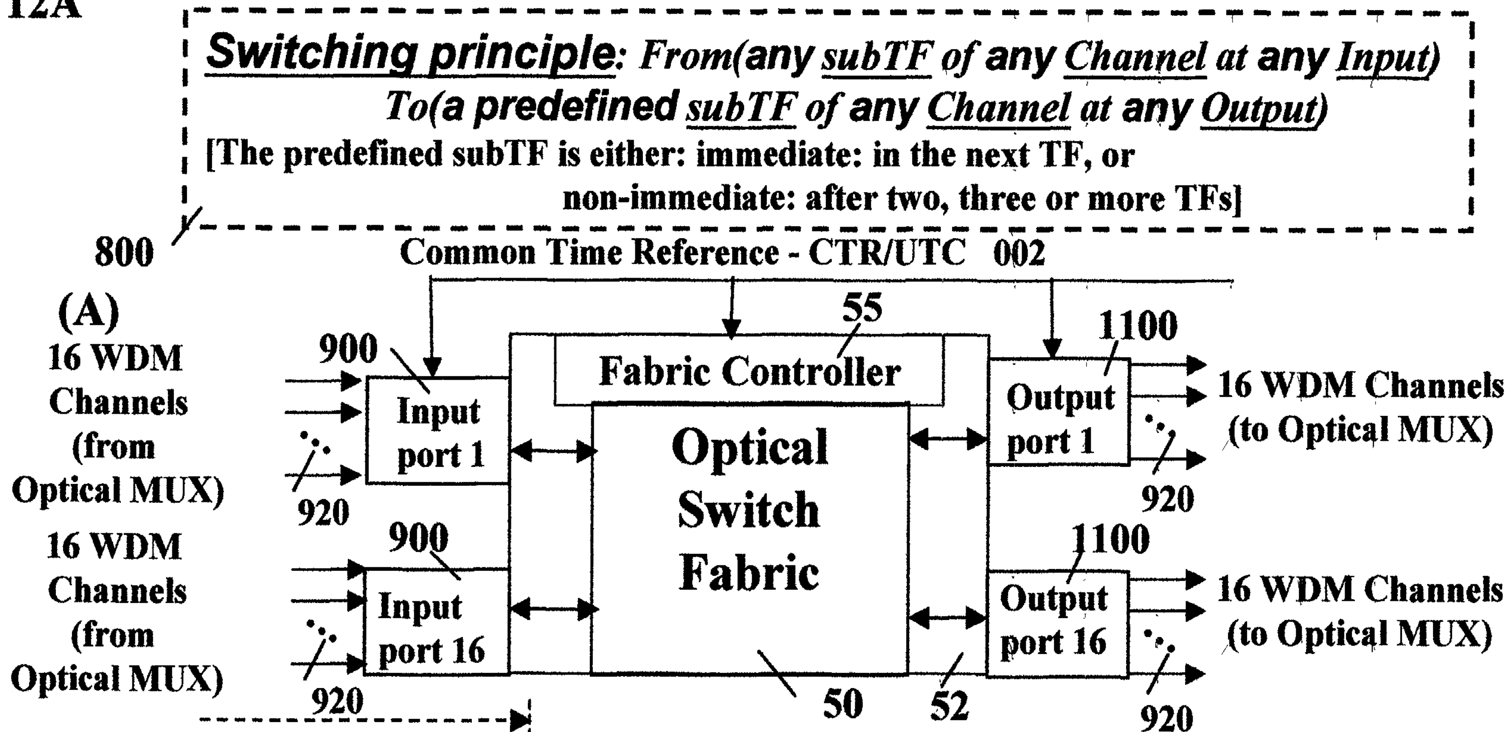


FIG. 12B

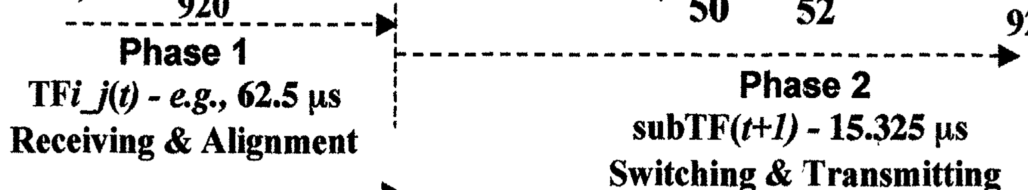


FIG. 12C

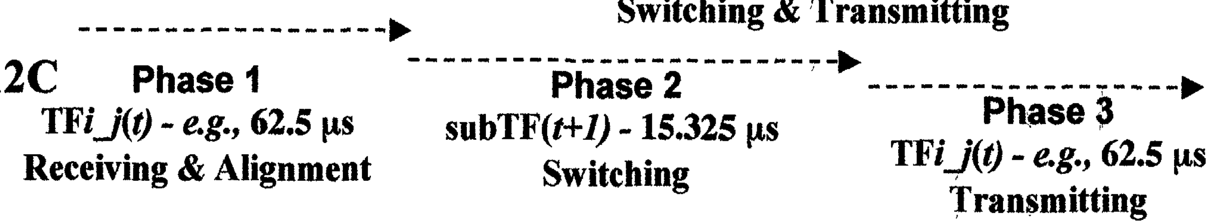
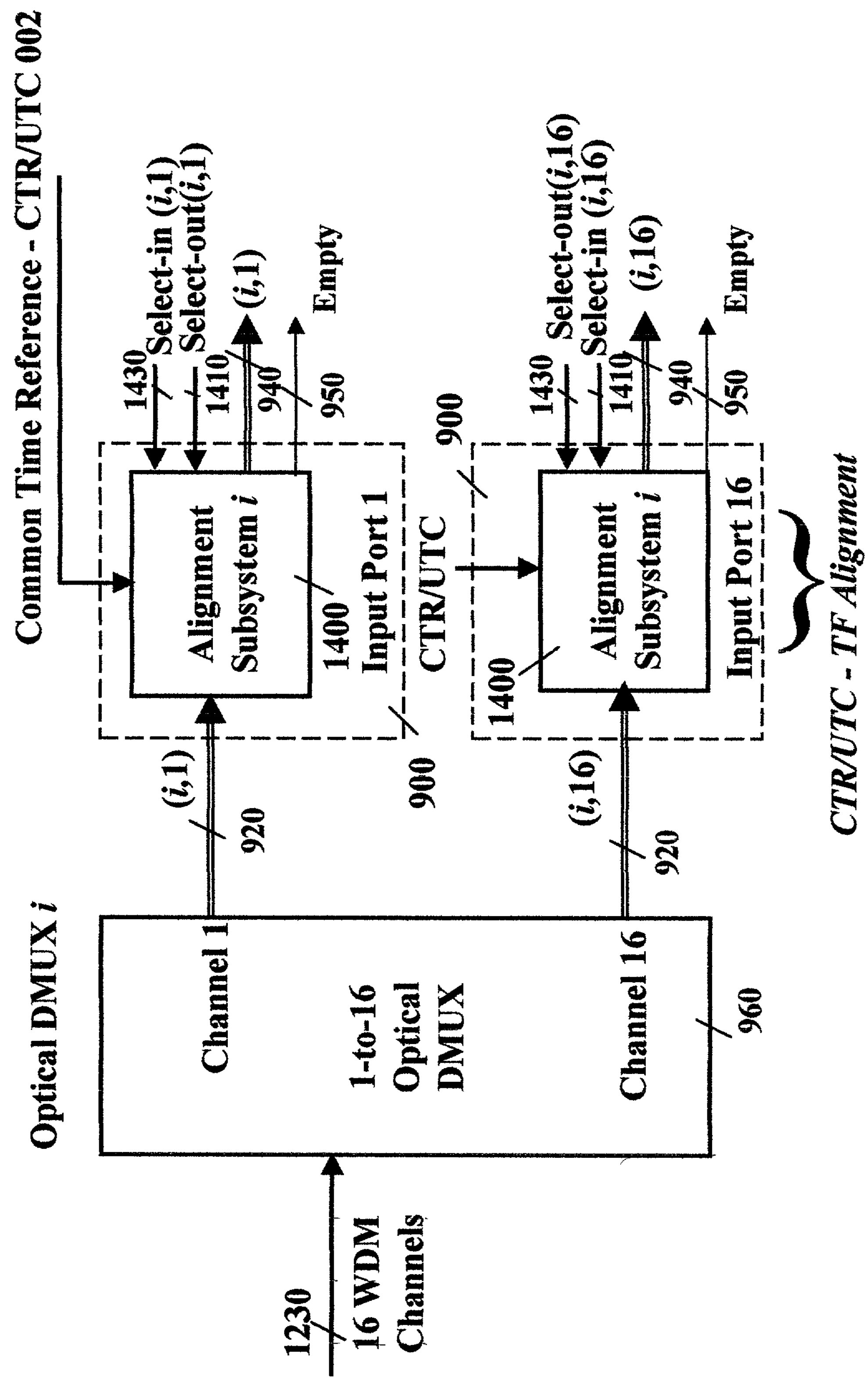


FIG. 13


Common Time Reference - CTR/UTC 002
Optical DMUX i
1-to-16 Optical DMUX
Channel 1
Channel 16
960
1230
16 WDM Channels
(i,1)
920
(i,16)
920
Alignment Subsystem i
1400
Input Port 1
900
Input Port 16
CTR/UTC
1430
Select-in (i,1)
1410
Select-out(i,1)
940
(i,1)
950
Empty
Select-out(i,16)
Select-in (i,16)
(i,16)
CTR/UTC - TF Alignment

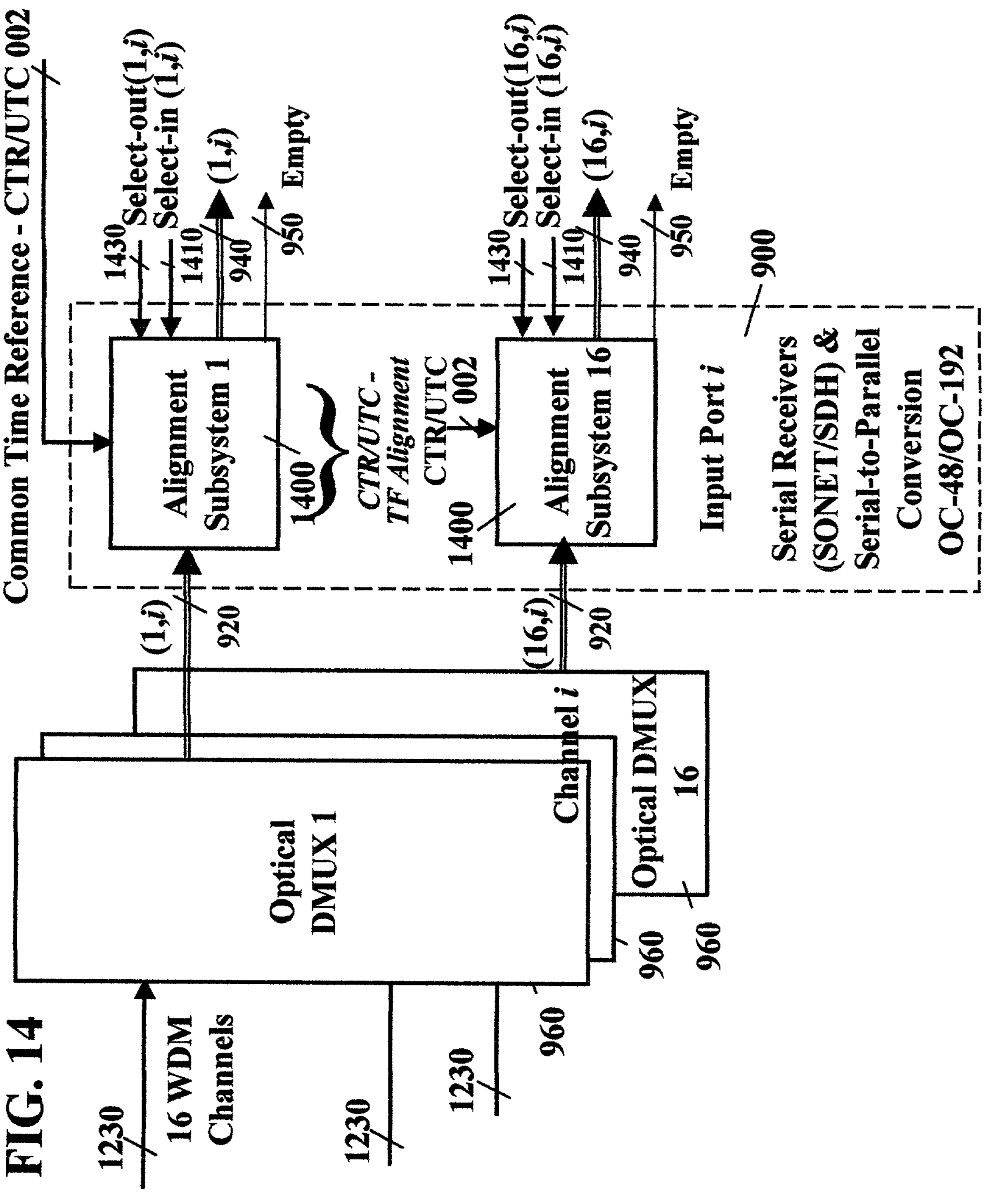

Common Time Reference - CTR/UTC 002
1430
Select-out(1,i)
Select-in (1,i)
1410
(1,i)
940
950
Empty
Alignment Subsystem 1
1400
CTR/UTC - TF Alignment
CTR/UTC 002
1430
Select-out(16,i)
Select-in (16,i)
1410
(16,i)
940
950
Empty
900
Alignment Subsystem 16
1400
Input Port i
Serial Receivers (SONET/SDH) & Serial-to-Parallel Conversion OC-48/OC-192
(1,i)
920
(16,i)
920
Channel i
Optical DMUX 1
Optical DMUX 16
960
960
960
1230
16 WDM Channels
1230
1230

FIG. 14

FIG. 15

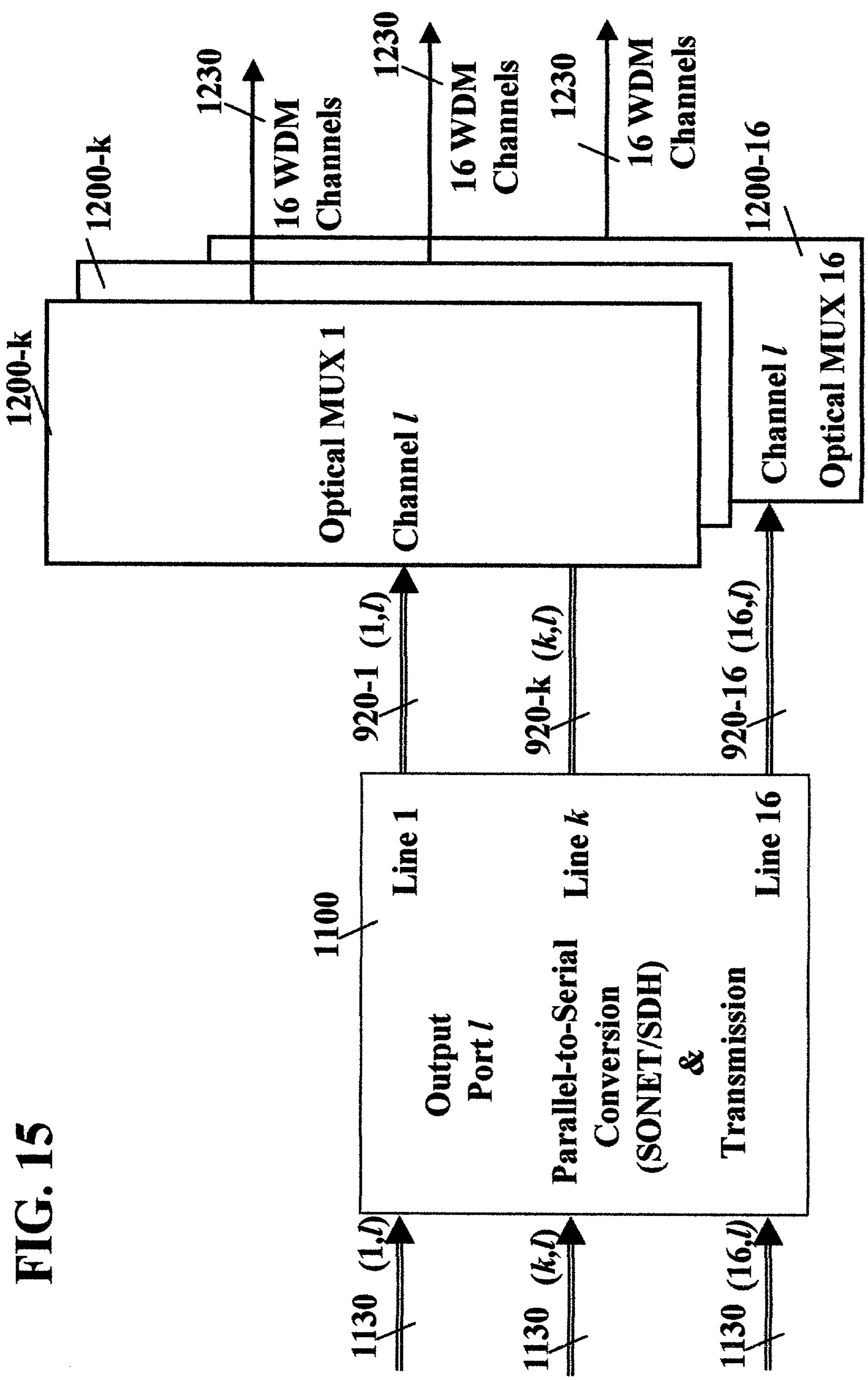

1200-k
1200-k
1200-16
1230
1230
1230
16 WDM Channels
16 WDM Channels
16 WDM Channels
Optical MUX 1
Channel l
Channel l
Optical MUX 16
920-1 (1,l)
920-k (k,l)
920-16 (16,l)
1100
Line 1
Line k
Line 16
Output Port l
Parallel-to-Serial Conversion (SONET/SDH) & Transmission
1130 (1,l)
1130 (k,l)
1130 (16,l)

FIG. 16

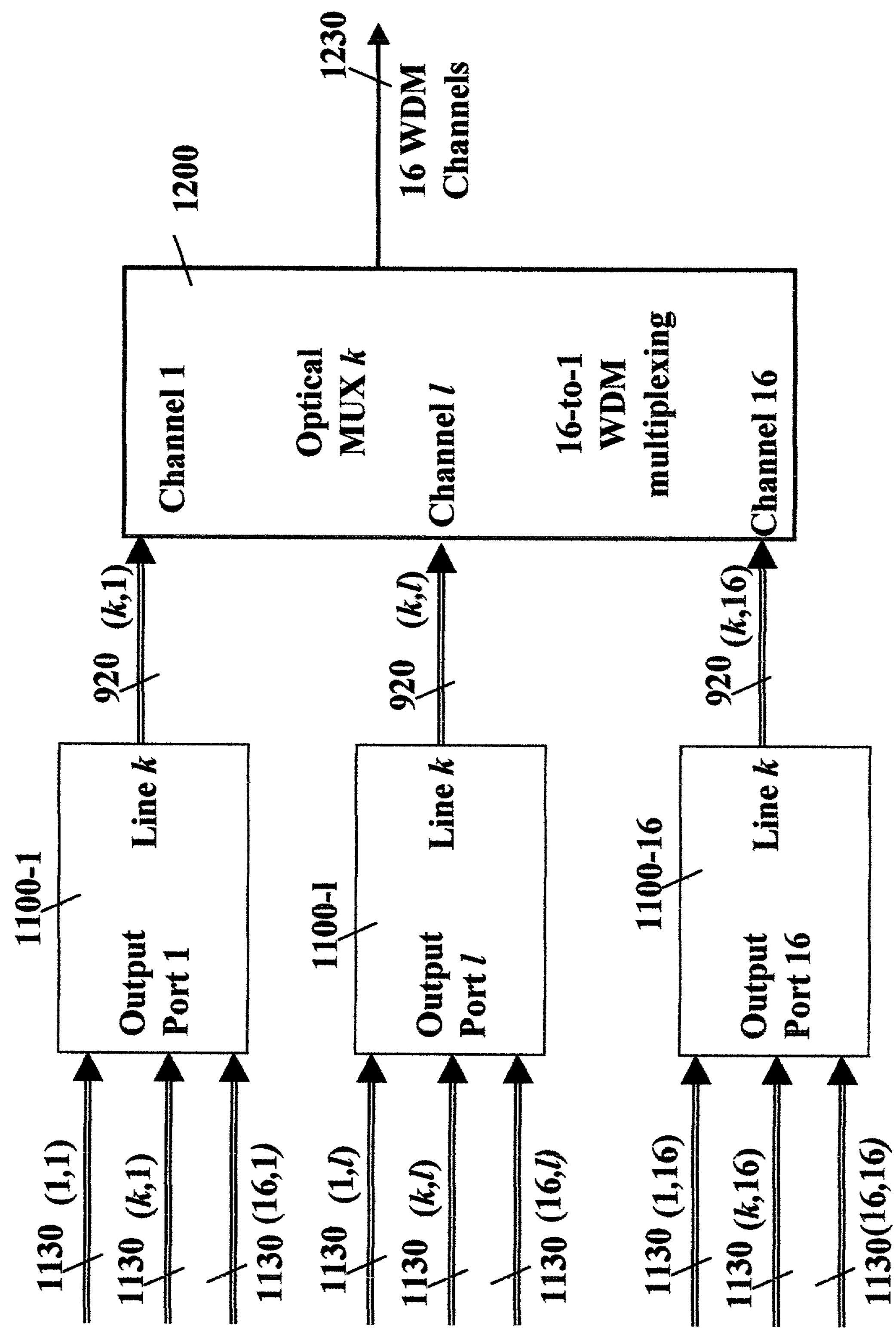

1130 (1,1)
1130 (k,1)
1130 (16,1)
1130 (1,l)
1130 (k,l)
1130 (16,l)
1130 (1,16)
1130 (k,16)
1130(16,16)
1100-1
Output Port 1
Line k
1100-1
Output Port l
Line k
1100-16
Output Port 16
Line k
920 (k,1)
920 (k,l)
920 (k,16)
1200
Channel 1
Optical MUX k
Channel l
16-to-1 WDM multiplexing
Channel 16
1230
16 WDM Channels

FIG. 17

N: number of input/output channels. E.g., N=256

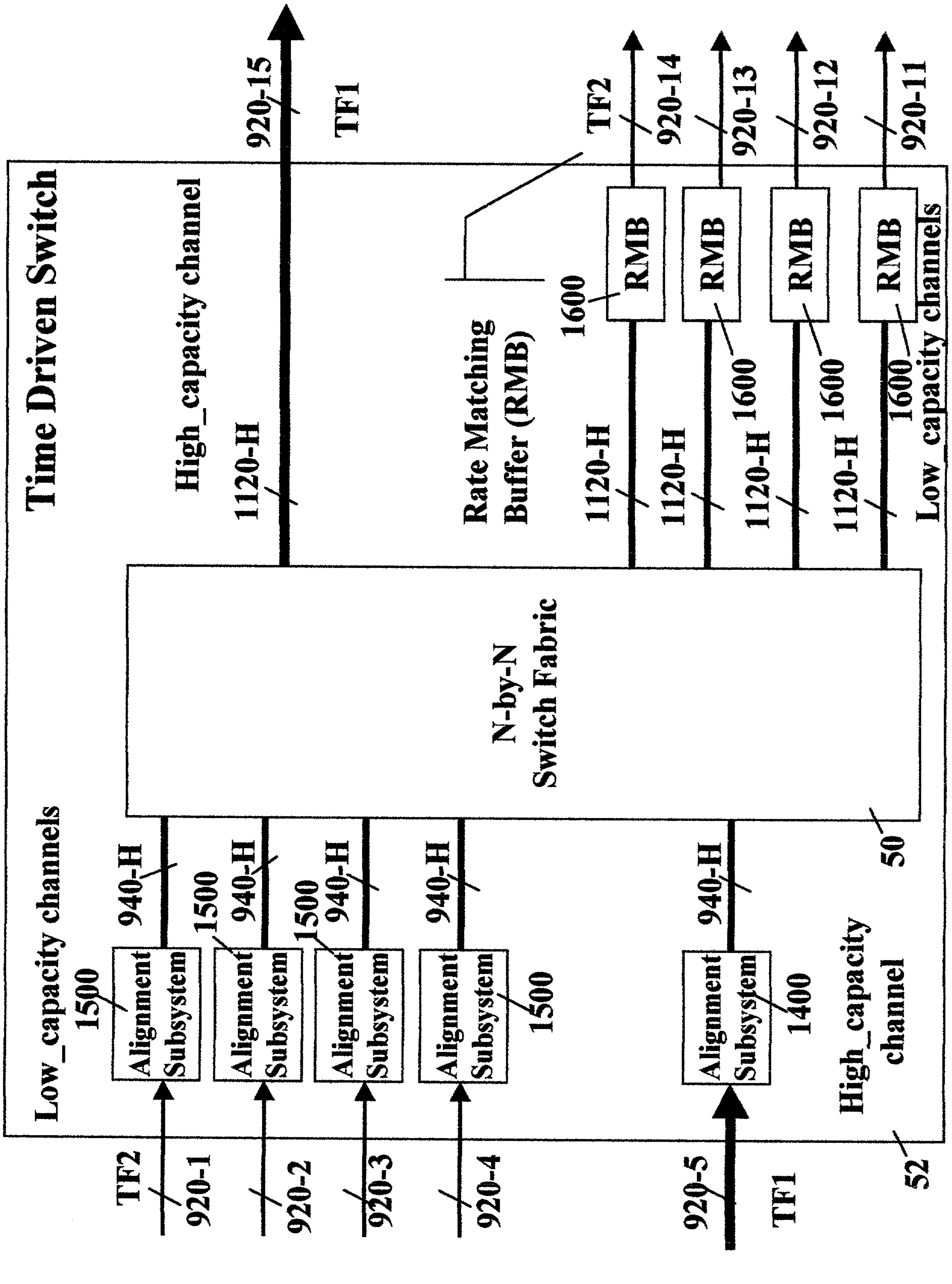
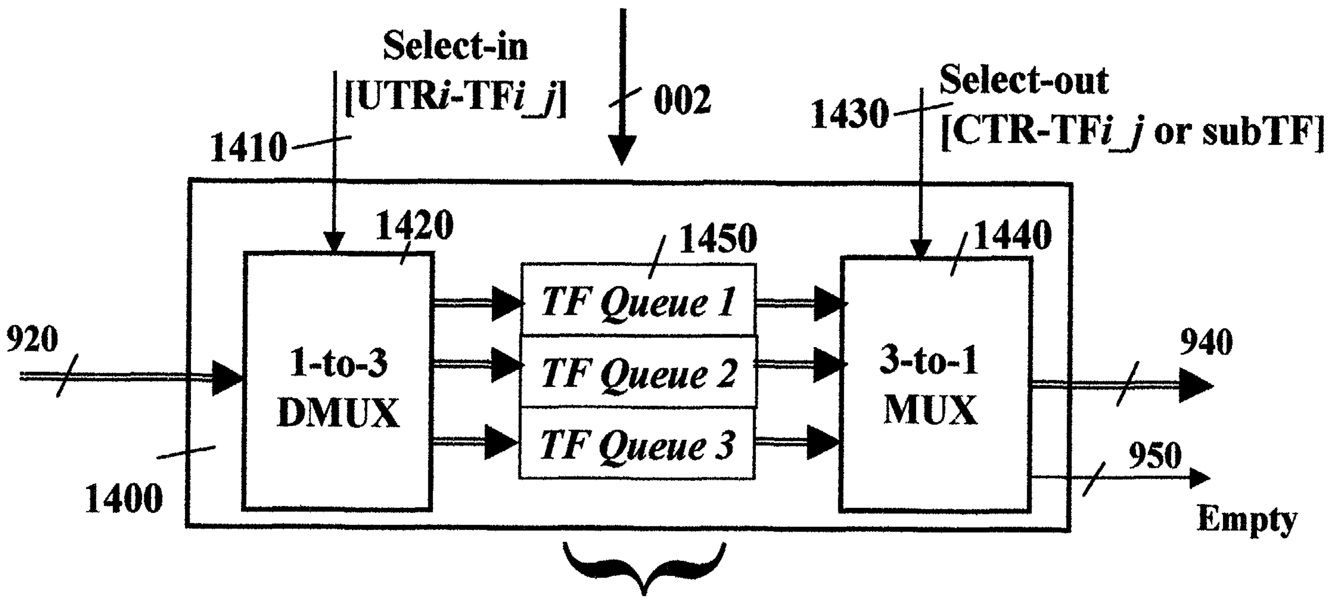


FIG. 18

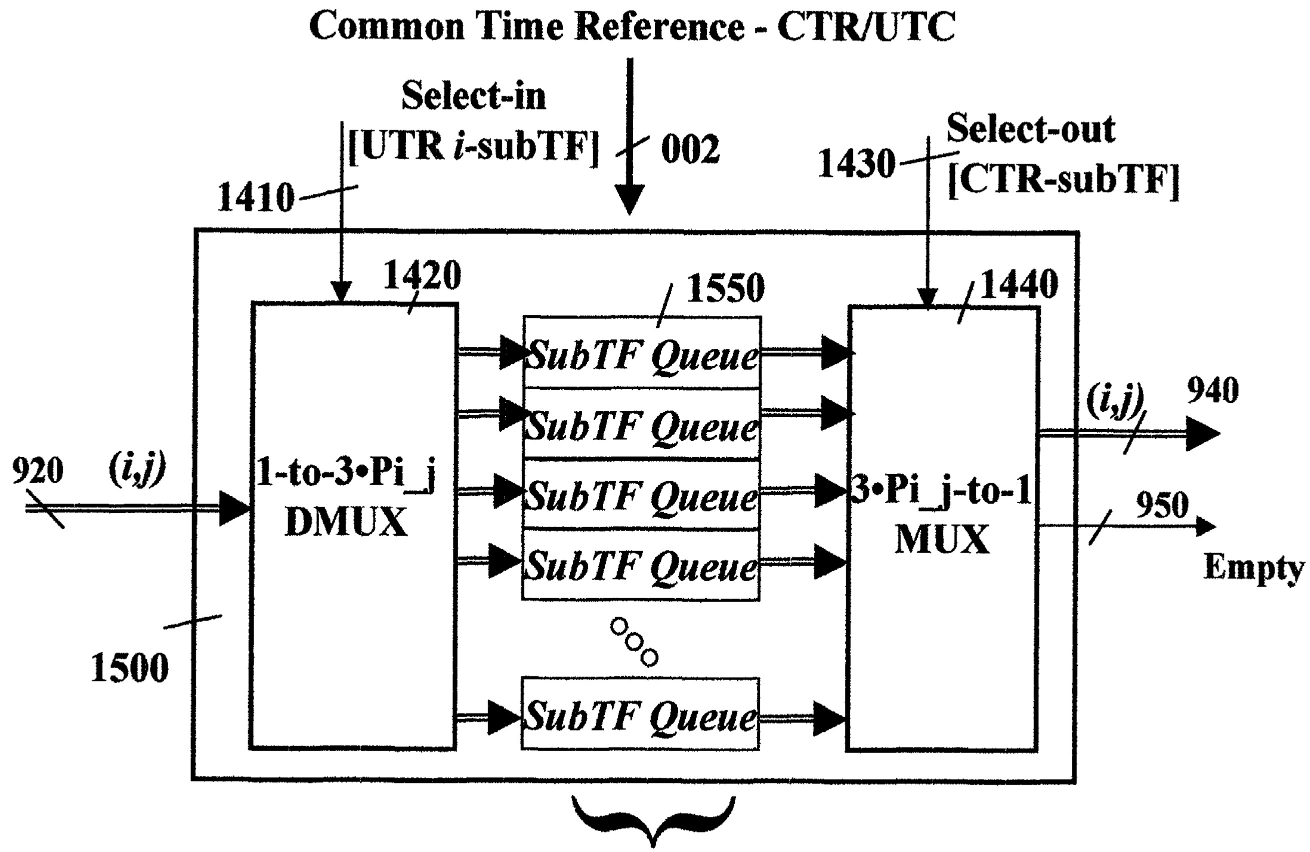
TF*i_j*: Time frame duration on channel *j* at Input Interface *i*.
UTR*i*: UTR on link connected to Input Interface *i*
Common Time Reference - CTR/UTC



Alignment Subsystem for Channel *j* at Input Interface *i*
with a Plurality of Time Frame Queues

FIG. 19

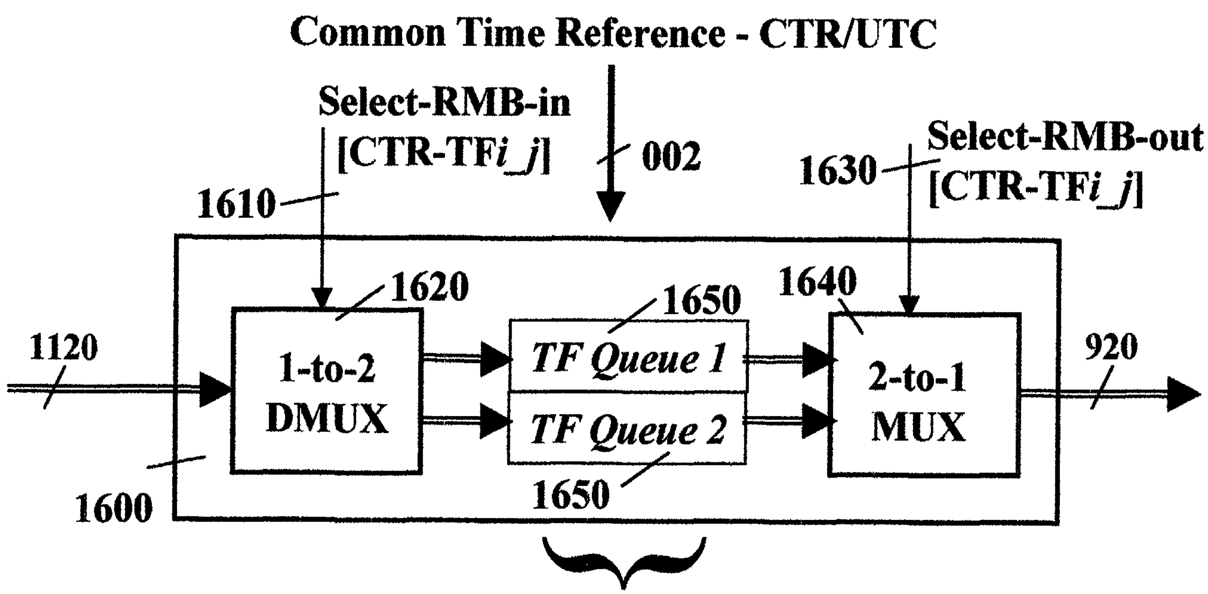
TFi_j: Time frame duration on channel j at Input Interface i.
UTR i: UTR on link connected to Input Interface i
Pi_j = TFi_j/subTF



Alignment Subsystem for *high capacity* Channel *j* at Input Interface *i*
with a Plurality of <u>Sub-Time Frame Queues</u>

FIG. 20

TF*i_j*: Time frame duration on channel *j* at Input Interface *i*.
UTR*i*: UTR on link connected to Input Interface *i*



Rate Matching Buffer for Channel *j* at Output Interface *i*
with a Plurality of <u>Time Frame Queues</u>
(Also single buffer with dual access memory with single phase switching and forwarding)

FIG. 21

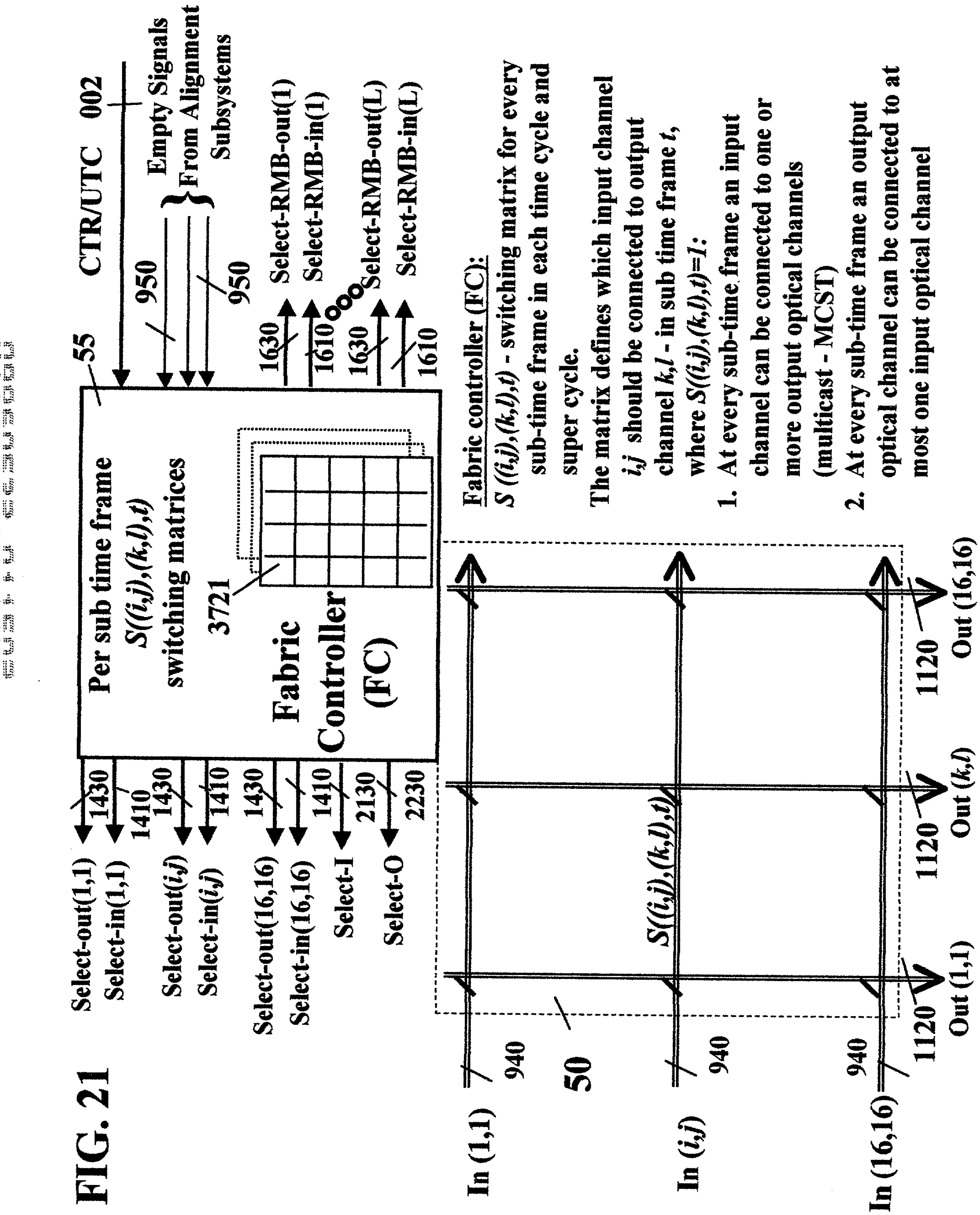
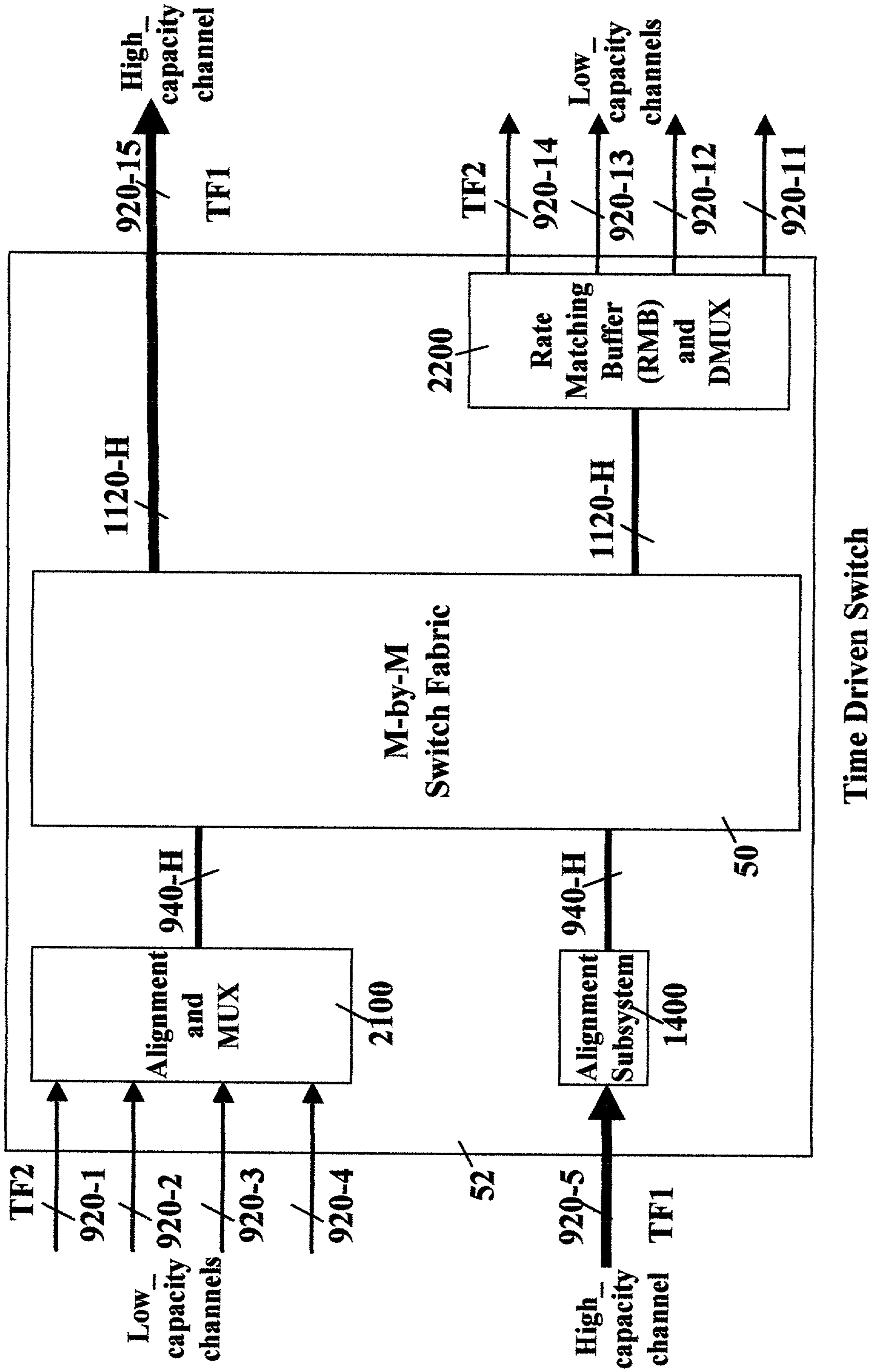

CTR/UTC 002
Empty Signals From Alignment Subsystems
950
950
55
Select-RMB-out(1)
Select-RMB-in(1)
Select-RMB-out(L)
Select-RMB-in(L)
1630
1610
1630
1610
Per sub time frame
S((i,j),(k,l),t)
switching matrices
3721
Fabric Controller (FC)
Select-out(1,1)
Select-in(1,1)
Select-out(i,j)
Select-in(i,j)
Select-out(16,16)
Select-in(16,16)
Select-I
Select-O
1430
1410
1430
1410
1430
1410
2130
2230
Fabric controller (FC):
S ((i,j),(k,l),t) - switching matrix for every sub-time frame in each time cycle and super cycle.
The matrix defines which input channel i,j should be connected to output channel k,l - in sub time frame t, where S((i,j),(k,l),t)=1:
1. At every sub-time frame an input channel can be connected to one or more output optical channels (multicast - MCST)
2. At every sub-time frame an output optical channel can be connected to at most one input optical channel
S((i,j),(k,l),t)
In (1,1)
In (i,j)
In (16,16)
940
940
940
50
1120
1120
1120
Out (1,1)
Out (k,l)
Out (16,16)

FIG. 22

N: number of input/output channels. E.g., N=256
M • High_capacity = N_high • High_capacity + N_low • Low_capacity
M<N



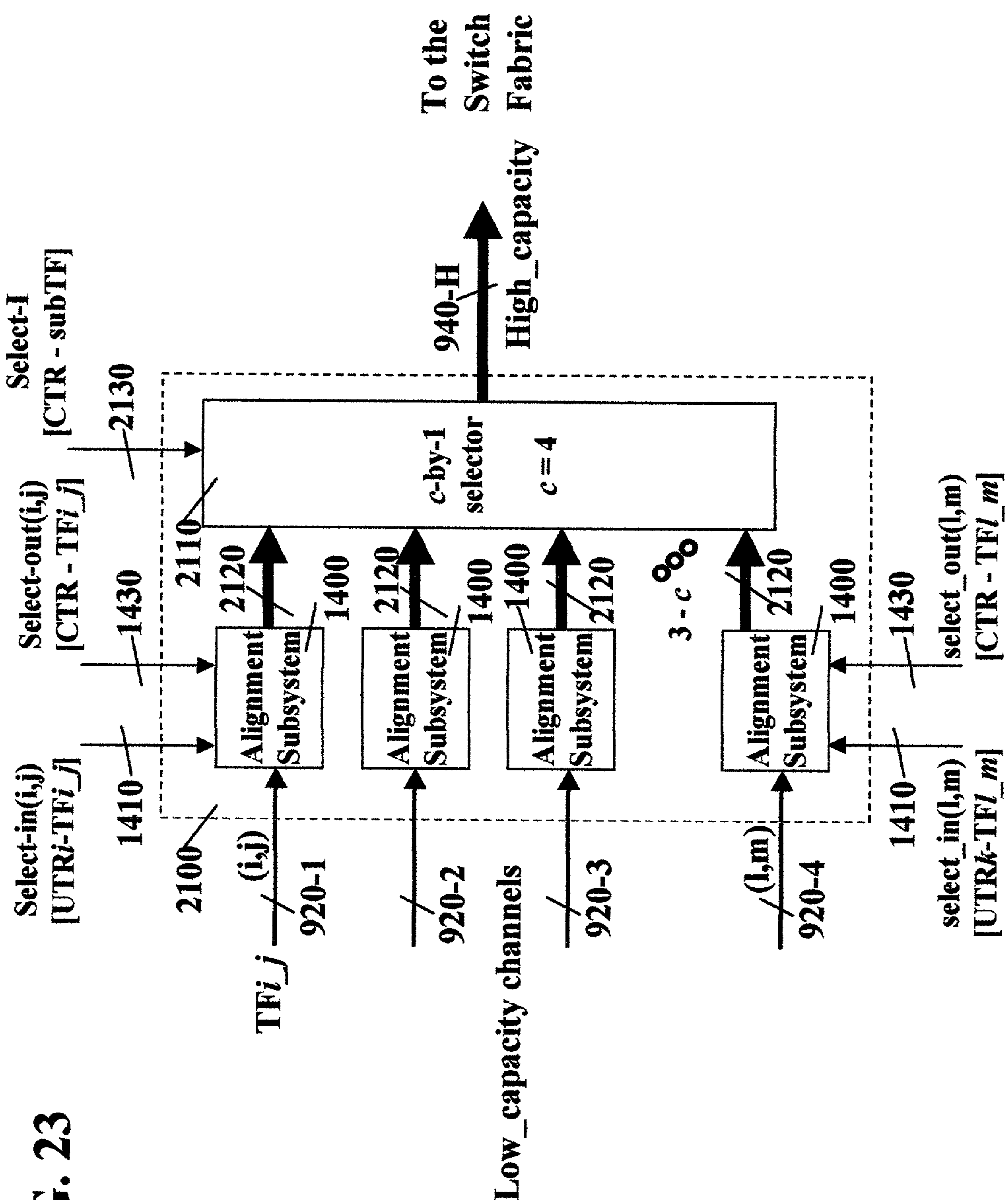

Select-in(i,j)
[UTRi-TFi_j]
1410
Select-out(i,j)
[CTR - TFi_j]
1430
Select-I
[CTR - subTF]
2130
2100
2110
2120
1400
Alignment Subsystem
c-by-1 selector
c = 4
3 - c
940-H
High_capacity
To the Switch Fabric
TFi_j
(i,j)
920-1
920-2
920-3
(l,m)
920-4
Low_capacity channels
select_in(l,m)
[UTRk-TFl_m]
select_out(l,m)
[CTR - TFl_m]

FIG. 23

FIG. 24

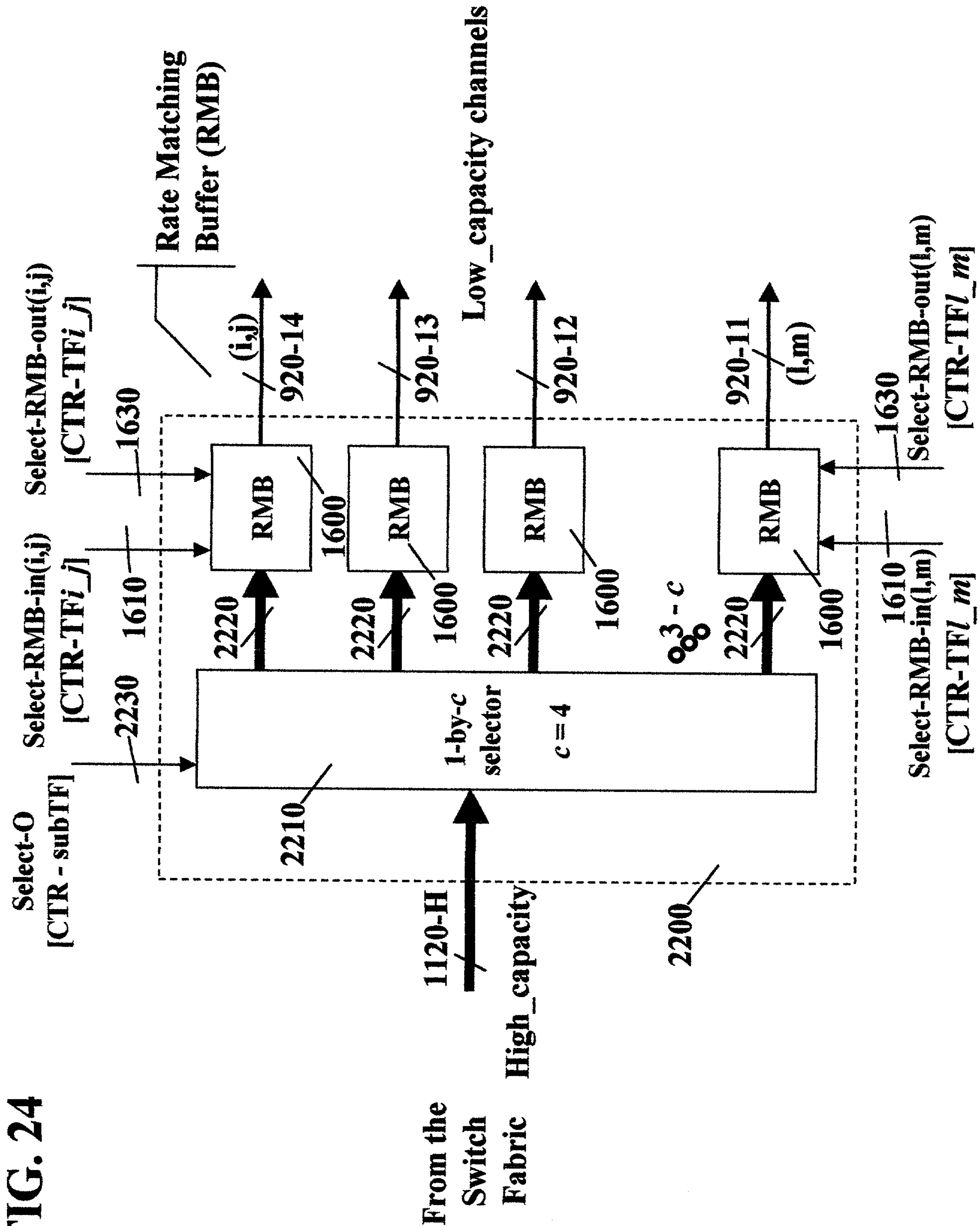

From the Switch Fabric
High_capacity
1120-H
Select-O [CTR - subTF]
2230
2210
1-by-c selector
c = 4
2200
Select-RMB-in(i,j) [CTR-TFi_j]
1610
Select-RMB-out(i,j) [CTR-TFi_j]
1630
2220
RMB
1600
3 - c
Select-RMB-in(l,m) [CTR-TFl_m]
Select-RMB-out(l,m) [CTR-TFl_m]
920-14
(i,j)
920-13
920-12
920-11
(l,m)
Rate Matching Buffer (RMB)
Low_capacity channels

FIG. 25

N: number of input/output channels. E.g., N=256
L • Low_capacity = N_high • High_capacity + N_low • Low_capacity
L > N

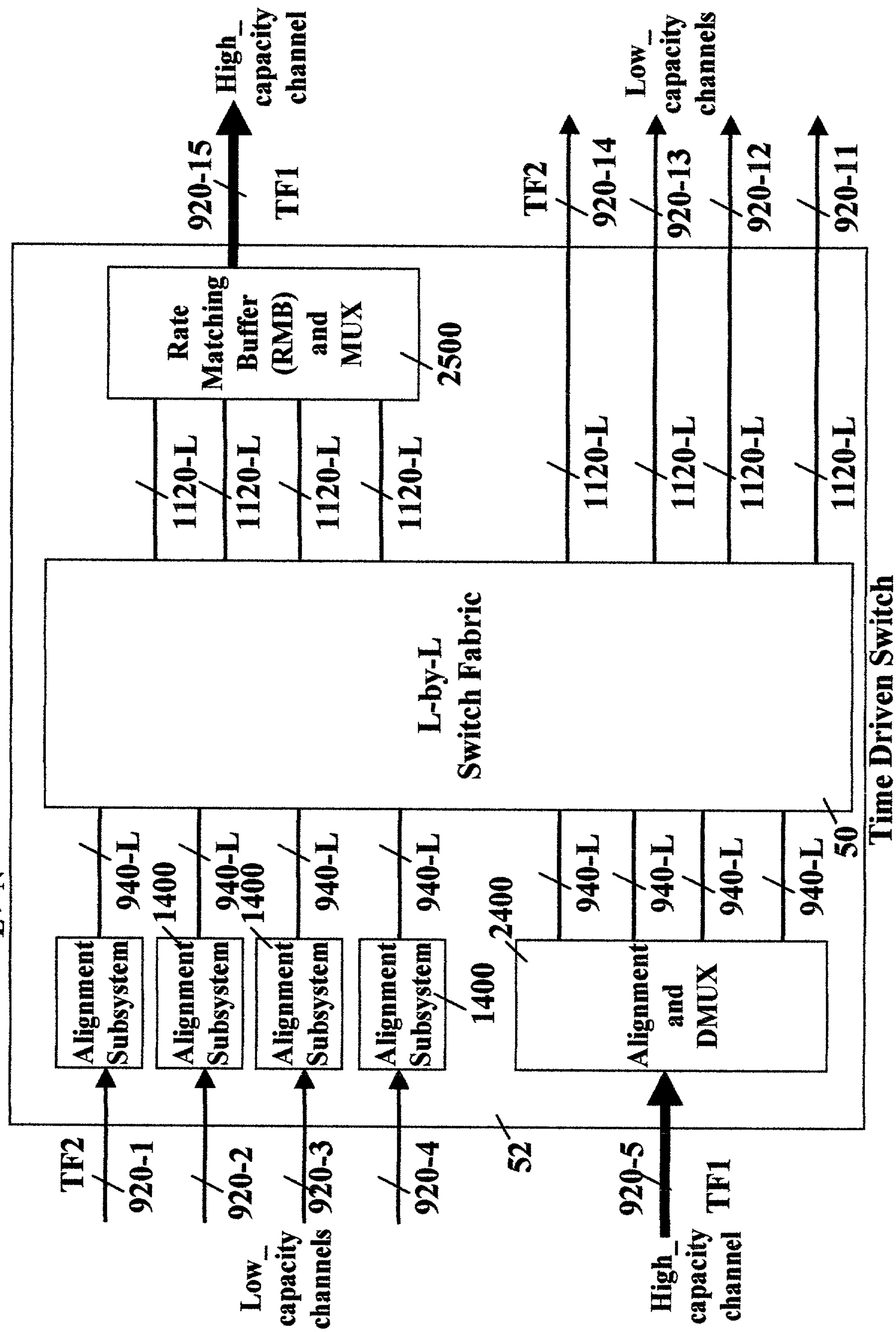
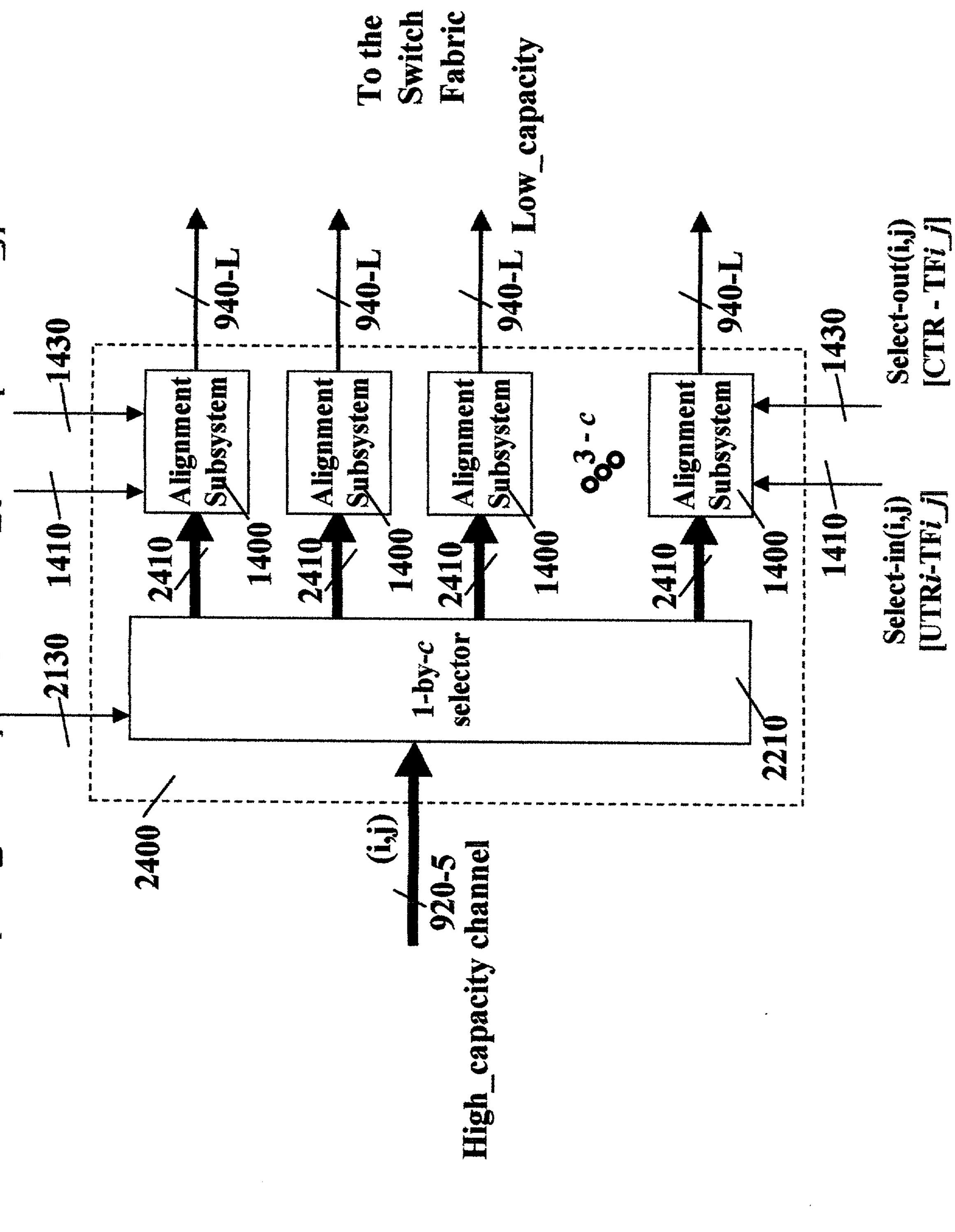


FIG. 26


Select-I
[UTRi_j - subTF]
Select-in(i,j)
[UTRi-TFi_j]
Select-out(i,j)
[CTR - TFi_j]
2400
2130
1410
1430
1-by-c
selector
2210
2410
1400
Alignment
Subsystem
940-L
To the
Switch
Fabric
Low_capacity
3 - c
(i,j)
920-5
High_capacity channel

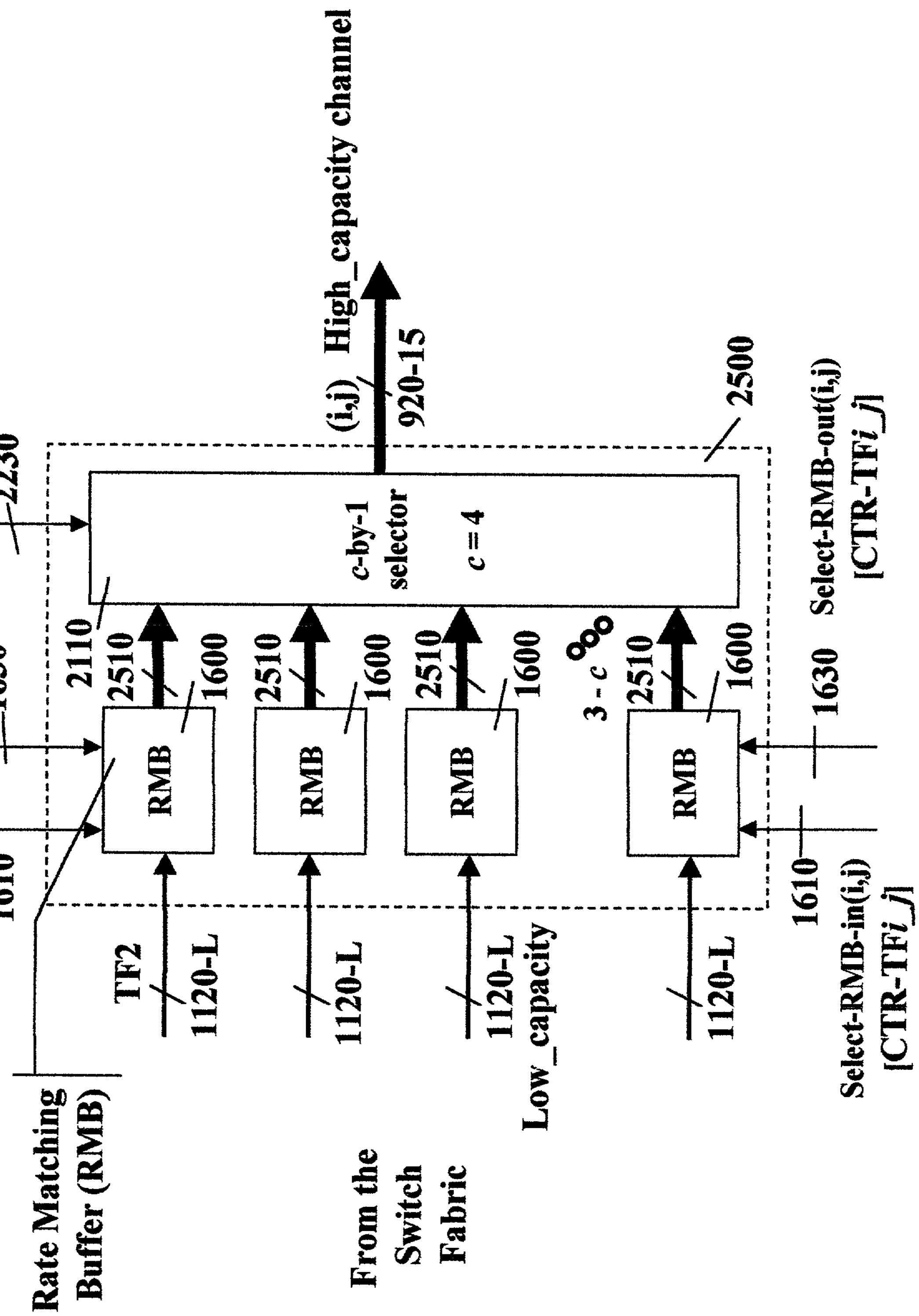

Rate Matching Buffer (RMB)
From the Switch Fabric
Select-RMB-in(i,j) [CTR-TFi_j]
Select-RMB-out(i,j) [CTR-TFi_j]
Select-O [CTR - subTF]
1610
1630
2230
2110
TF2
1120-L
1120-L
1120-L
Low_capacity
1120-L
RMB
RMB
RMB
RMB
2510
1600
2510
1600
2510
1600
3 - c
2510
1600
c-by-1 selector
c = 4
2500
(i,j)
920-15
High_capacity channel
1630
1610
Select-RMB-out(i,j) [CTR-TFi_j]
Select-RMB-in(i,j) [CTR-TFi_j]

FIG. 27

FIG. 28

N: number of input/output channels. E.g., N=256
L • Low_capacity = N • High_capacity
L = c • N > N

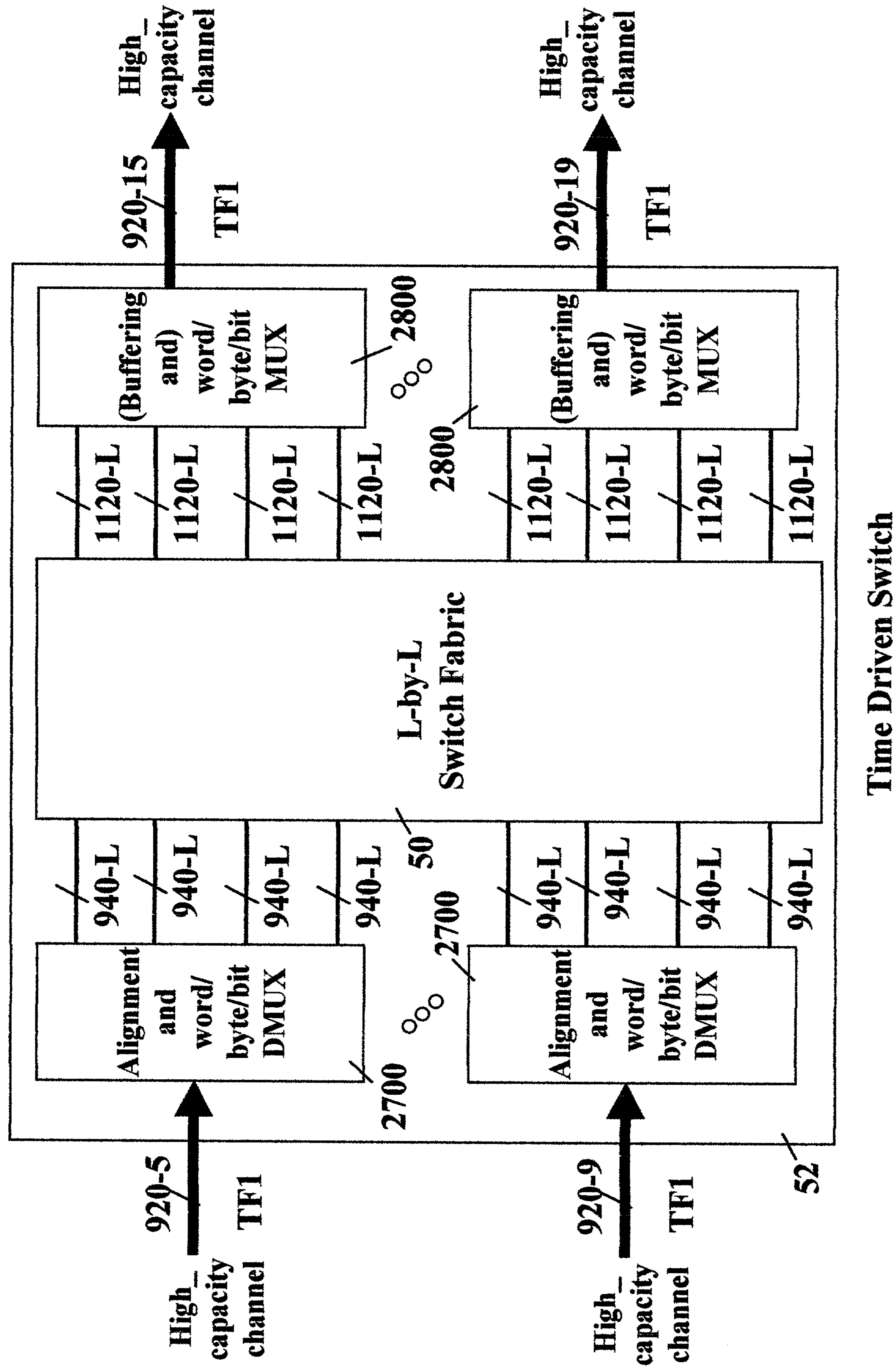


FIG. 29

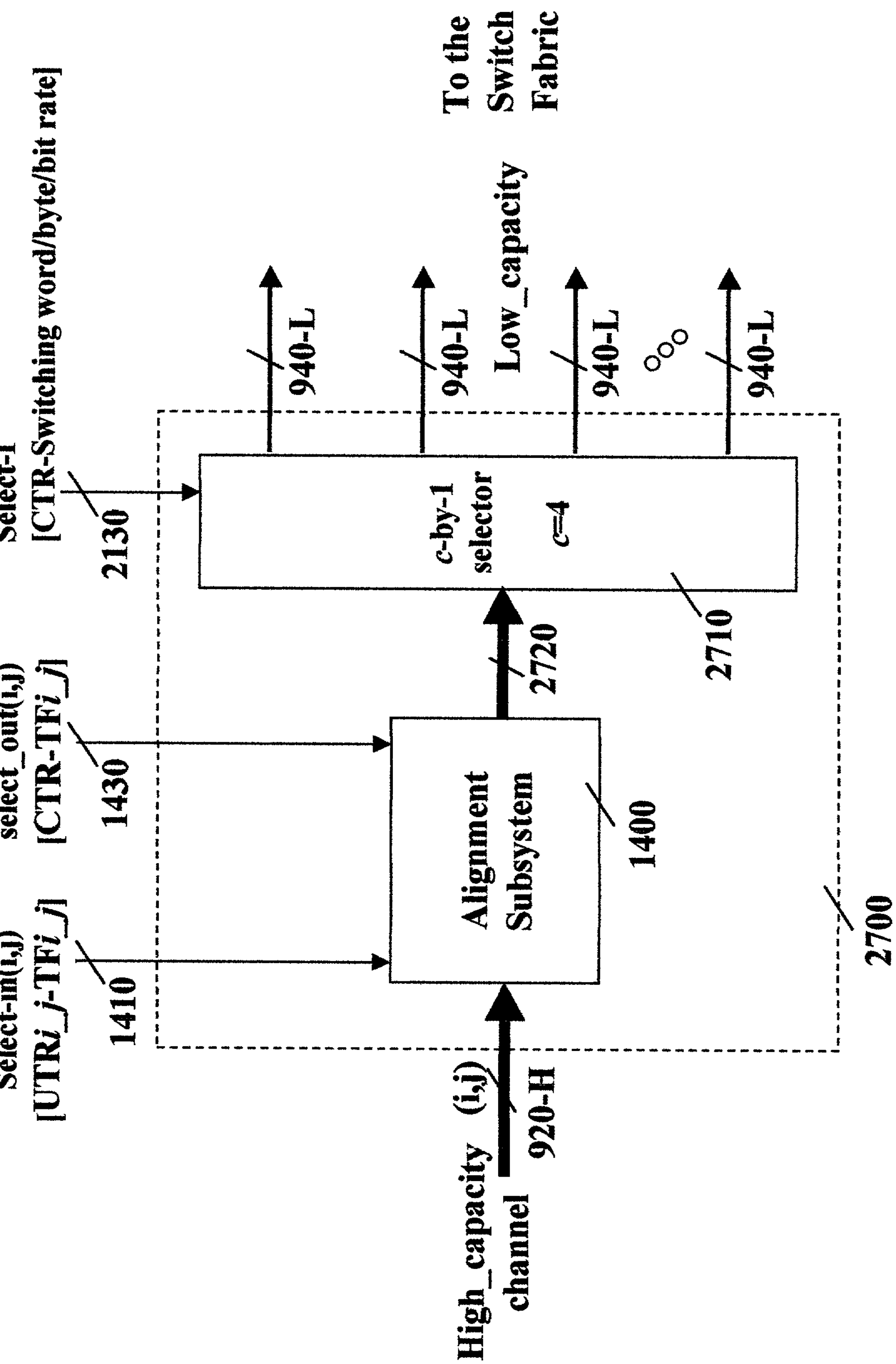
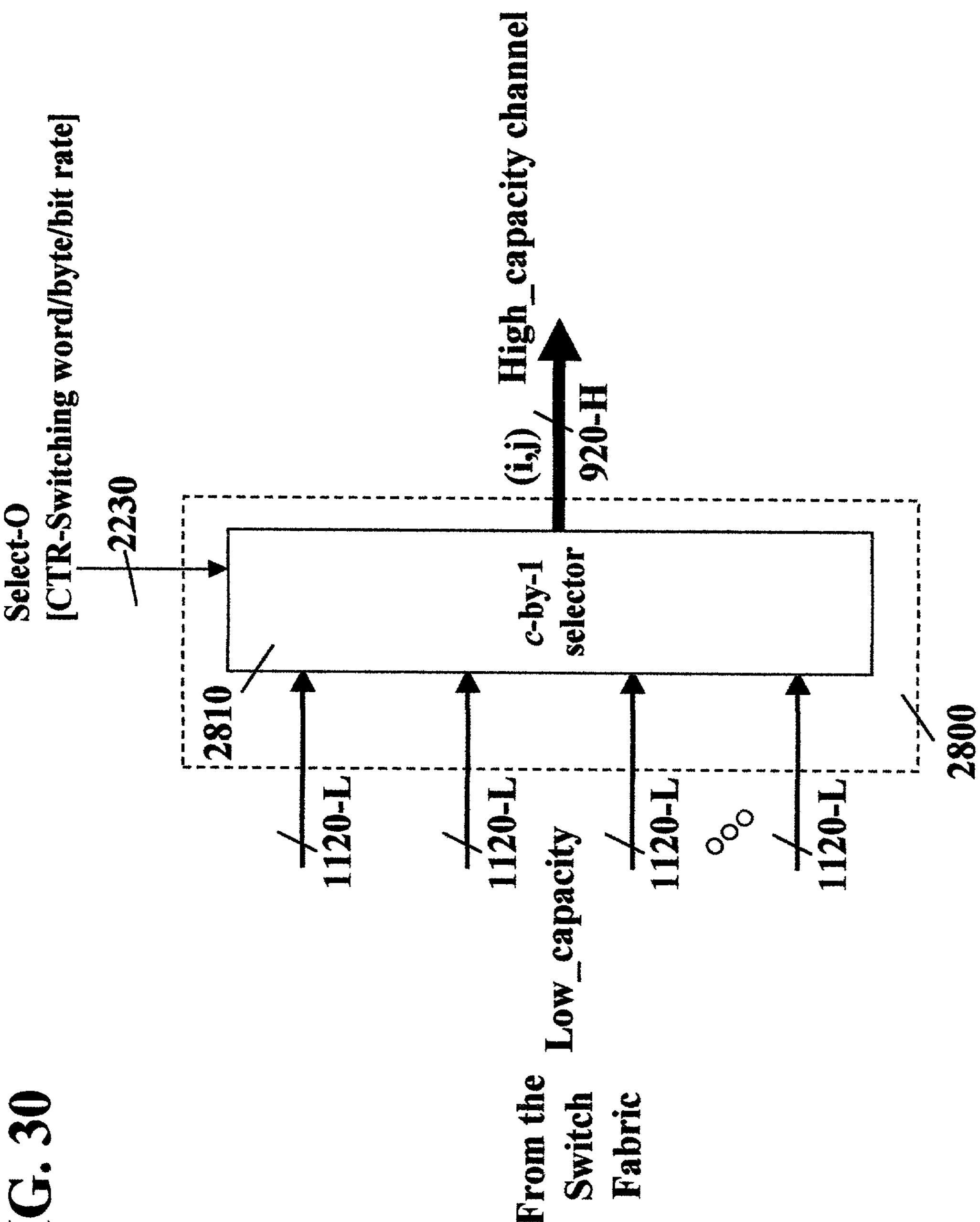

Select-in(i,j)
[UTRi_j-TFi_j]
1410
select_out(i,j)
[CTR-TFi_j]
1430
Select-I
[CTR-Switching word/byte/bit rate]
2130
High_capacity (i,j)
channel
920-H
Alignment
Subsystem
1400
2720
c-by-1
selector
c=4
2710
2700
940-L
940-L
940-L
940-L
Low_capacity
To the
Switch
Fabric

FIG. 30


Select-O
[CTR-Switching word/byte/bit rate]
2230
(i,j)
920-H
High_capacity channel
c-by-1
selector
2810
2800
1120-L
1120-L
1120-L
1120-L
From the
Switch
Fabric
Low_capacity

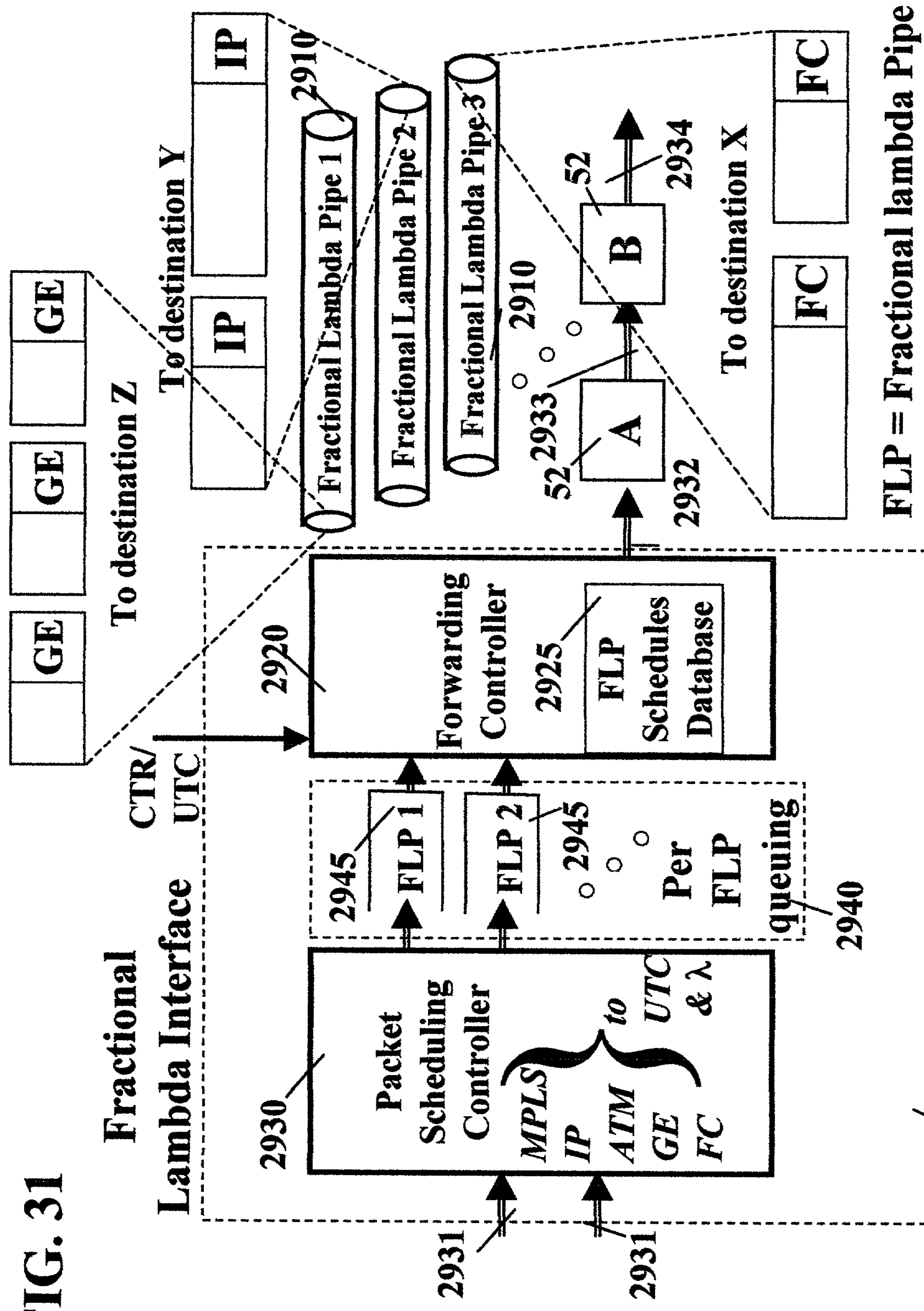

Fractional Lambda Interface
2930
Packet Scheduling Controller
MPLS
IP
ATM
GE
FC
to UTC & λ
2931
2931
2900
2945
FLP 1
FLP 2
2945
Per FLP queuing
2940
CTR/ UTC
2920
Forwarding Controller
2925
FLP Schedules Database
To destination Z
GE
GE
GE
To destination Y
IP
IP
2910
Fractional Lambda Pipe 1
Fractional Lambda Pipe 2
Fractional Lambda Pipe 3
2910
2933
52
A
2932
52
B
2934
To destination X
FC
FC
FLP = Fractional lambda Pipe

FIG. 31

FIG. 32

Channel Capacity		TF Duration	TF Size		STS-1s	TFs/s
51.84	STS- 1	250	1620	1512	2	4000
		500	3240	3024	4	2000
		1000	6480	6048	8	1000
155.52	STS- 3	125	2430	2268	3	8000
		250	4860	4536	6	4000
		500	9720	9072	12	2000
622.08	STS- 12	62.5	4860	4536	6	16000
		125	9720	9072	12	8000
		250	19440	18144	24	4000
2488.32	STS- 48	62.5	19440	18144	24	16000
		31.25	9720	9072	12	32000
		15.625	4860	4536	6	64000
9953.28	STS- 192	7.8125	9720	9072	12	128000
		15.625	19440	18144	24	64000
1000	GE	125	15625	15625	19.3	8000
		100	12500	12500	15.4	10000
		80	10000	10000	12.3	12500
10000	10GE	15.625	19531.25	19531.3	24.1	64000
		12.5	15625	15625	19.3	80000
		10	12500	12500	15.4	100000

FIG. 33

Ch Capacity		TF Dur.	TF Size	GE TFs	TFs/s
1000	**GE**	**80**	**10000**	**1.0**	**12500**
51.84	STS- 1	250	1512	0.15	4000
		500	3024	0.30	2000
		1000	6048	0.60	1000
155.5	STS- 3	125	2268	0.23	8000
		250	4536	0.45	4000
		500	9072	0.91	2000
622.1	STS- 12	62.5	4536	0.45	16000
		125	9072	0.91	8000
		250	18144	1.81	4000
2488	STS- 48	62.5	18144	1.81	16000
		31.25	9072	0.91	32000
		15.625	4536	0.45	64000
9953	STS- 192	7.8125	9072	0.91	128000
		15.625	18144	1.81	64000
10000	10GE	8	10000	1.00	125000
		16	20000	2.00	62500

FIG. 34

Ch Capacity		TF Dur.	TF Size	GE TFs	TFs/s
1000	**GE**	**62.5**	**7812.5**	**1.0**	**16000**
51.84	STS- 1	250	1512	0.19	4000
		500	3024	0.39	2000
		1000	6048	0.77	1000
155.52	STS- 3	125	2268	0.29	8000
		250	4536	0.58	4000
		500	9072	1.16	2000
622.08	STS- 12	62.5	4536	0.58	16000
		125	9072	1.16	8000
		250	18144	2.32	4000
2488.32	STS- 48	62.5	18144	2.32	16000
		31.25	9072	1.16	32000
		15.625	4536	0.58	64000
9953.28	STS- 192	7.8125	9072	1.16	128000
		15.625	18144	2.32	64000
10000	10GE	12.5	15625	2.00	80000
		25	31250	4.00	40000

FIG. 35

***TF Alignment of* UTR(j) *to* UTC -** **with three input queues - principle of operation:**

The same queue is not used simultaneously for:

1. Receiving data packets from the serial link, and

2. Forwarding data packets to the switch

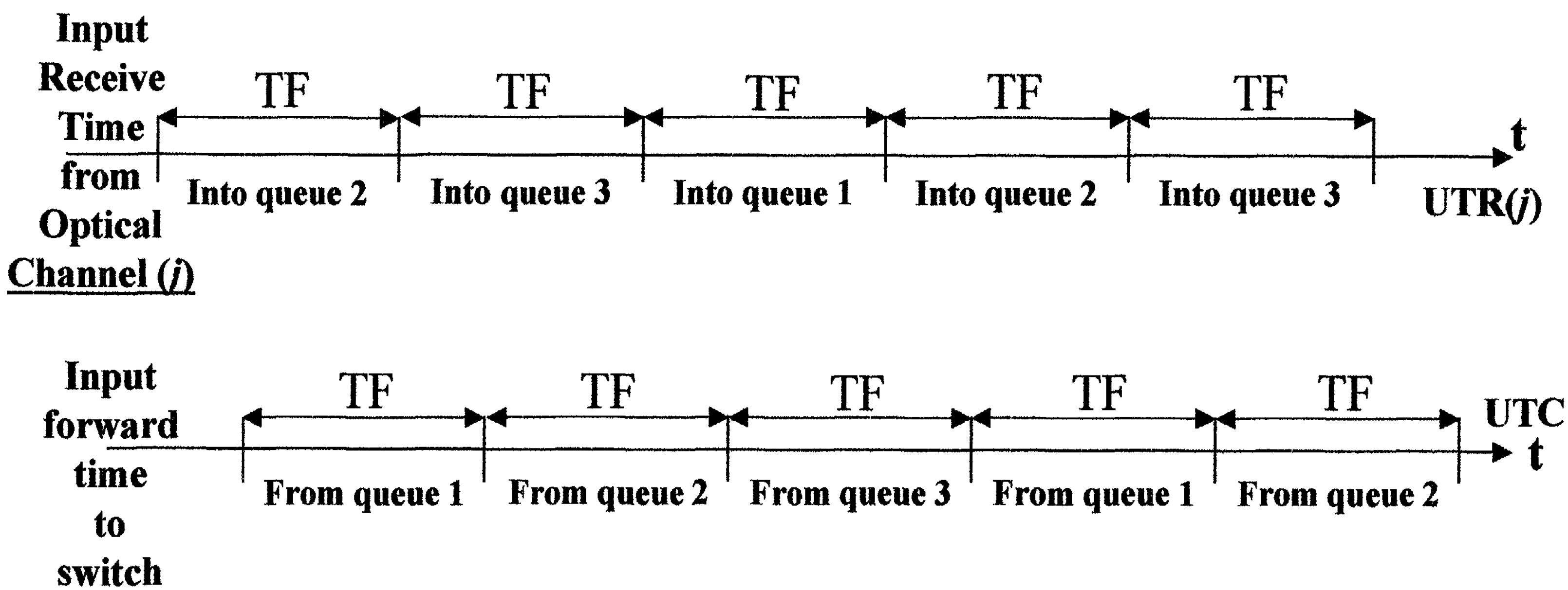
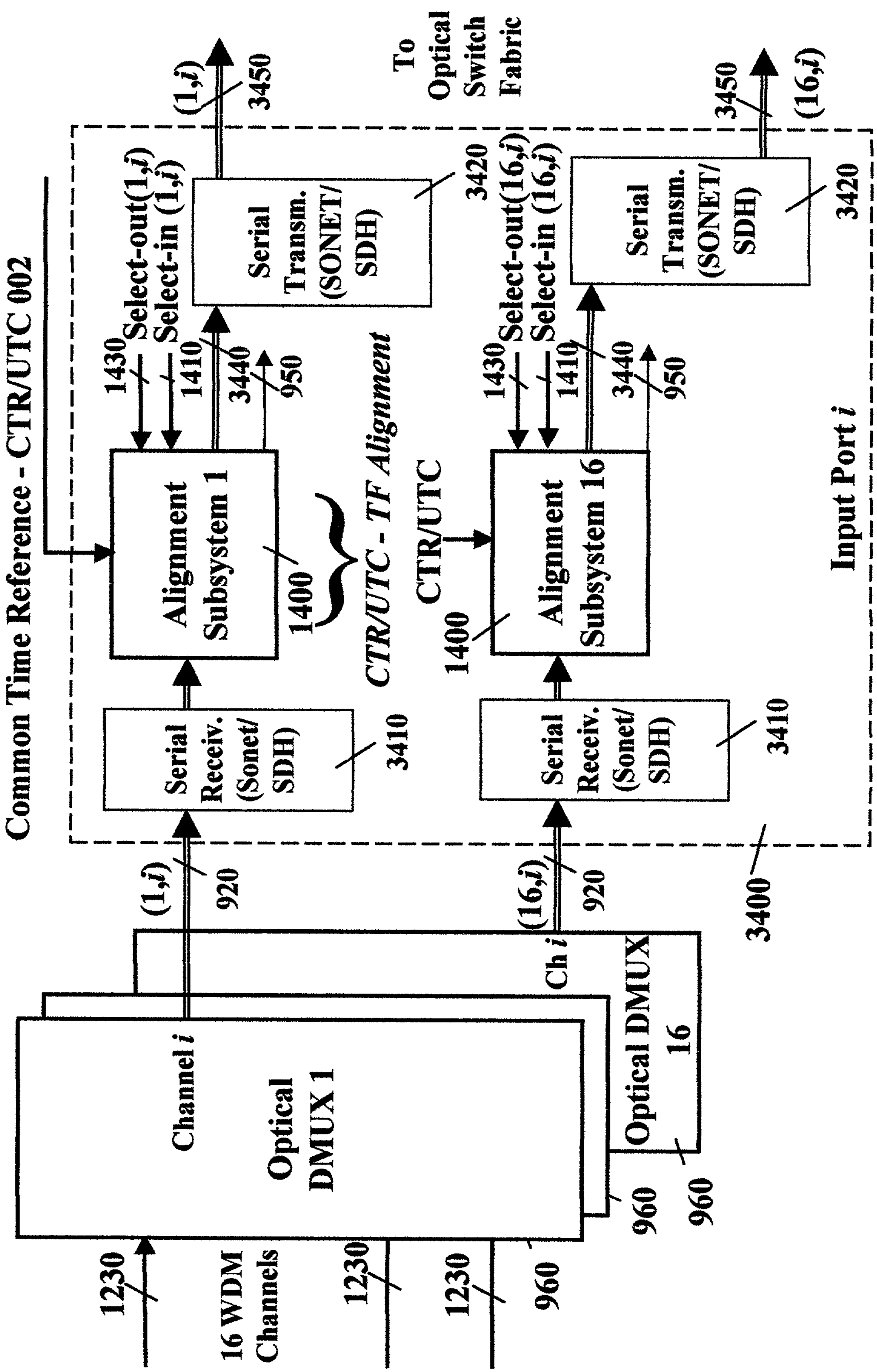


FIG. 36


Common Time Reference - CTR/UTC 002
16 WDM Channels
1230
1230
1230
Optical DMUX 1
Channel i
960
960
960
Optical DMUX 16
Ch i
(1,i)
920
(16,i)
920
3400
Input Port i
Serial Receiv. (Sonet/SDH)
3410
Serial Receiv. (Sonet/SDH)
3410
Alignment Subsystem 1
1400
CTR/UTC - TF Alignment
CTR/UTC
Alignment Subsystem 16
1400
1430
1410
3440
950
Select-out(1,i)
Select-in (1,i)
1430
1410
3440
950
Select-out(16,i)
Select-in (16,i)
Serial Transm. (SONET/SDH)
3420
Serial Transm. (SONET/SDH)
3420
(1,i)
3450
3450
(16,i)
To Optical Switch Fabric

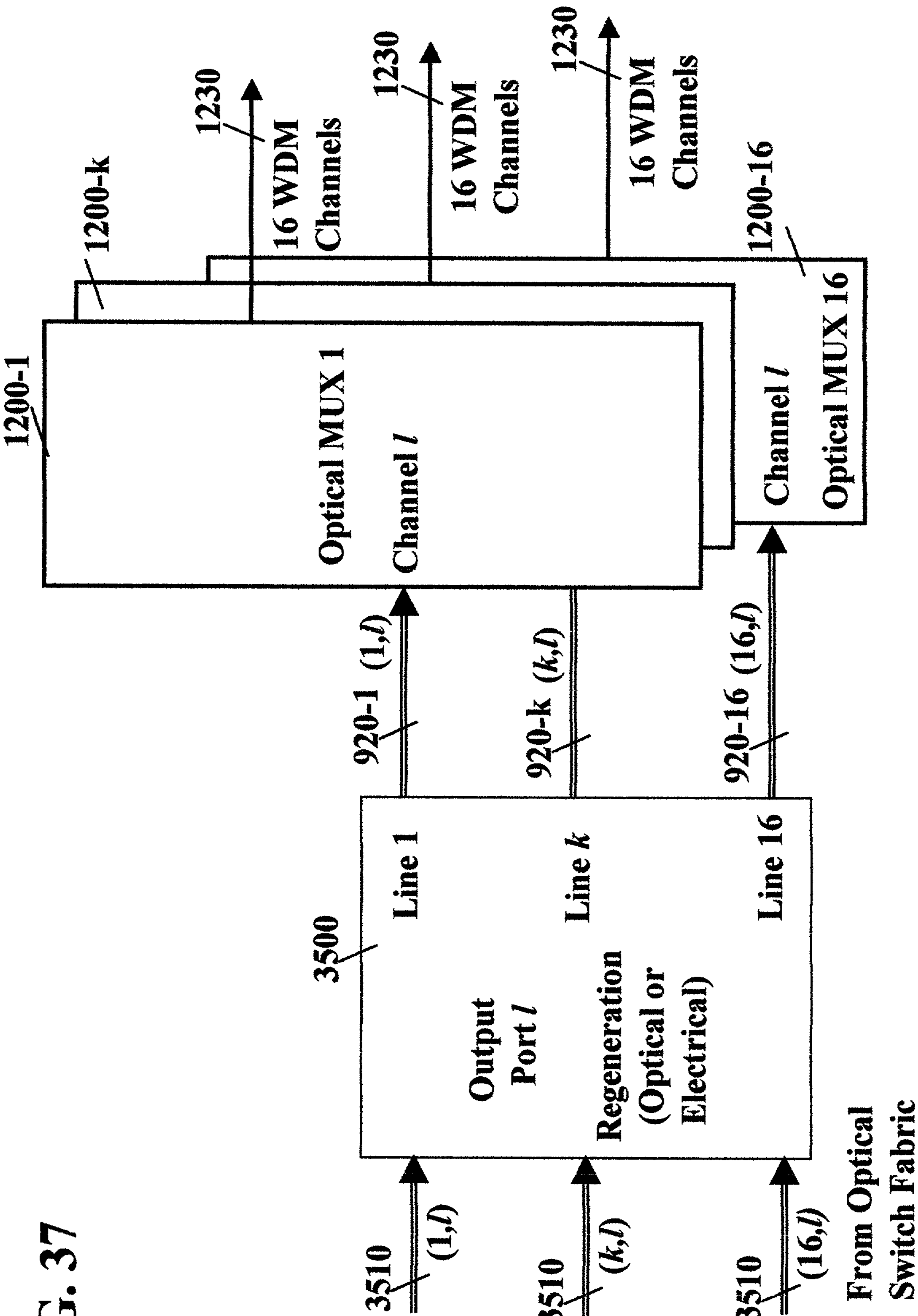
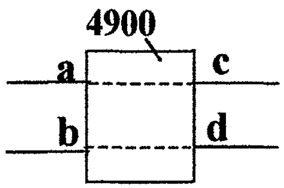

3510
(1,l)
3510
(k,l)
3510
(16,l)
From Optical Switch Fabric
3500
Output Port l
Regeneration (Optical or Electrical)
Line 1
Line k
Line 16
920-1 (1,l)
920-k (k,l)
920-16 (16,l)
1200-1
Optical MUX 1
Channel l
1200-k
1200-16
Channel l
Optical MUX 16
1230
16 WDM Channels
1230
16 WDM Channels
1230
16 WDM Channels

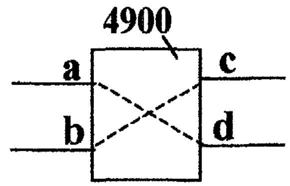
FIG. 37

FIG. 38A



Straight Connection of a
2-by-2 Optical Switching Block

FIG. 38B



Cross Connection of a
2-by-2 Optical Switching Block

FIG. 38C

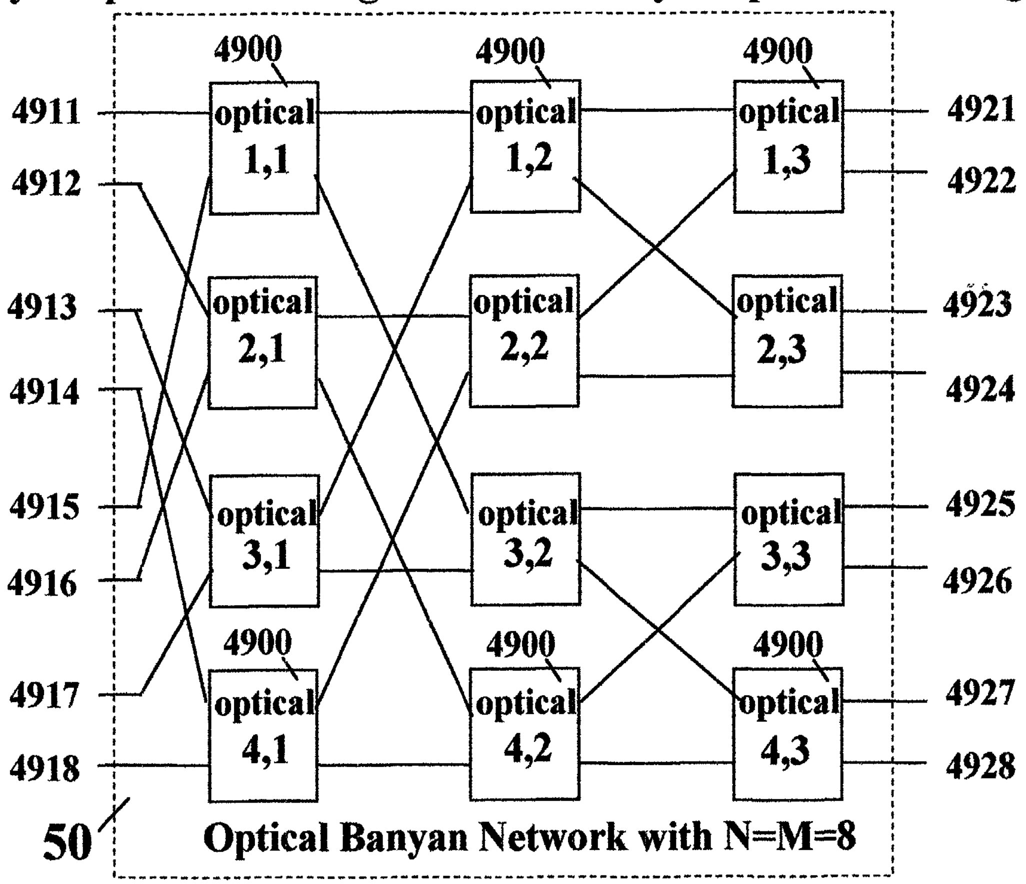
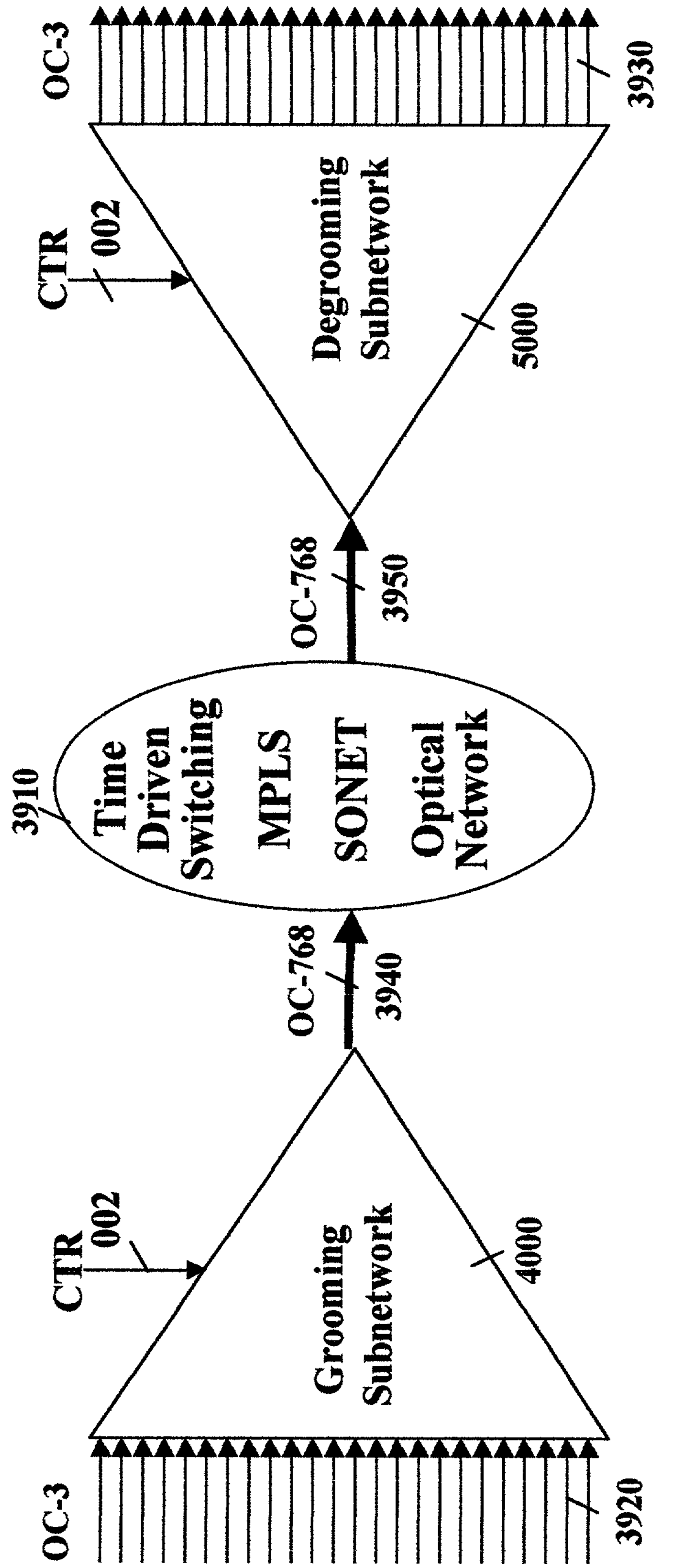


FIG. 39


OC-3
3920
CTR
002
Grooming Subnetwork
4000
OC-768
3940
3910
Time Driven Switching
MPLS
SONET
Optical Network
OC-768
3950
CTR
002
Degrooming Subnetwork
5000
OC-3
3930

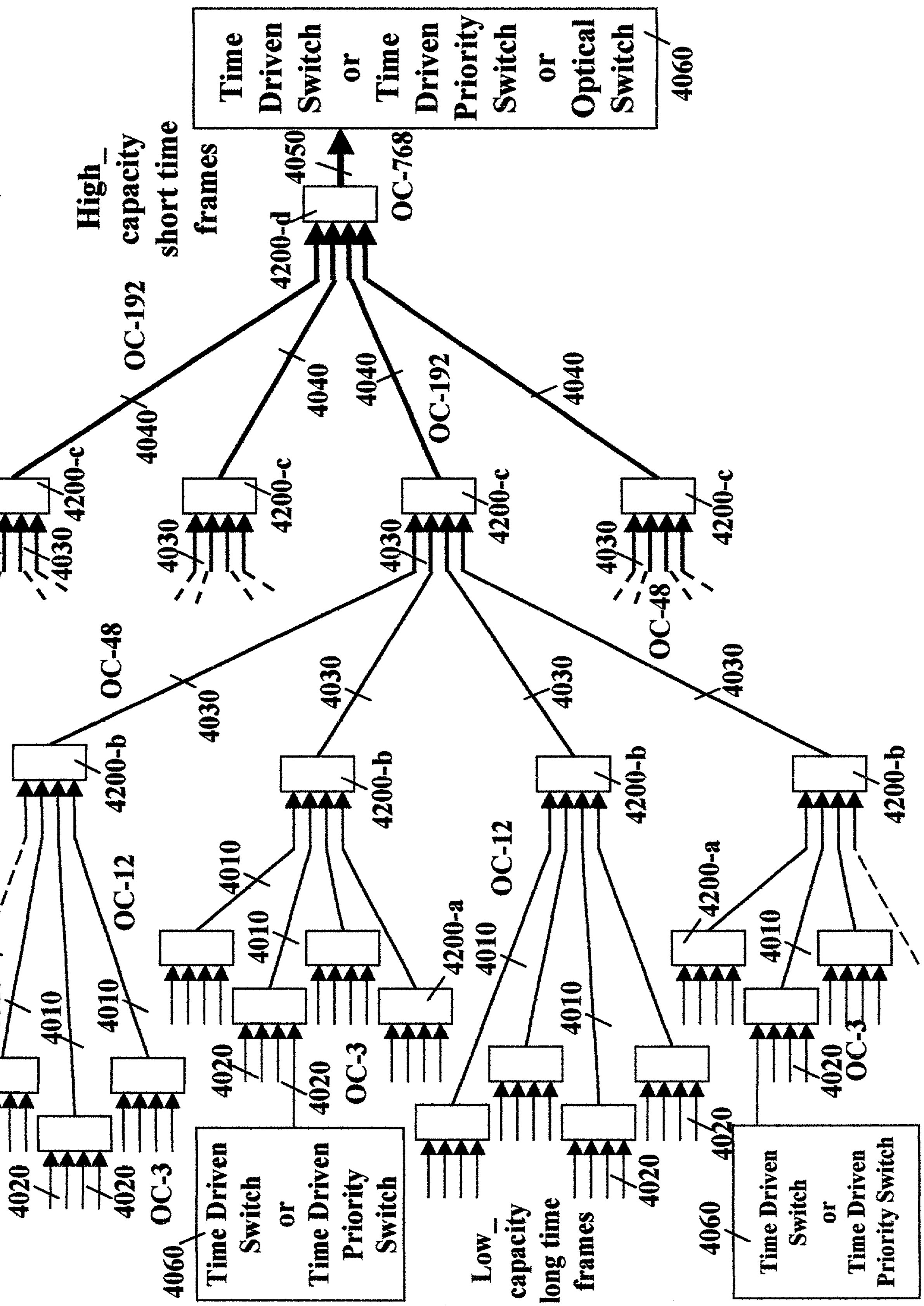

Time Driven Switch or Time Driven Priority Switch or Optical Switch
4060
High_ capacity short time frames
4050
OC-768
4200-d
OC-192
4040
4200-c
4030
OC-48
4200-b
OC-12
4010
4200-a
4020
OC-3
Time Driven Switch or Time Driven Priority Switch
Low_ capacity long time frames

FIG. 40

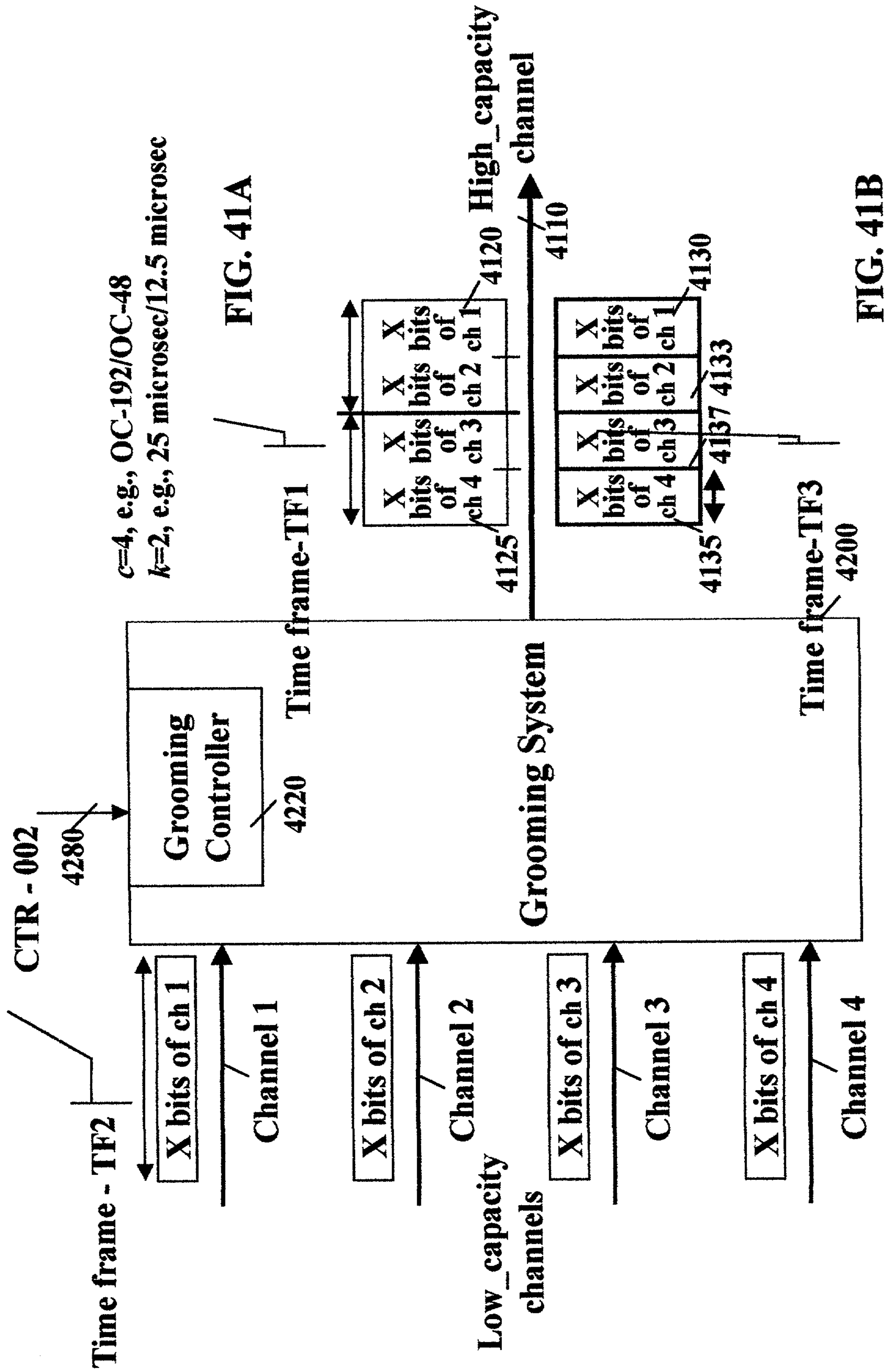
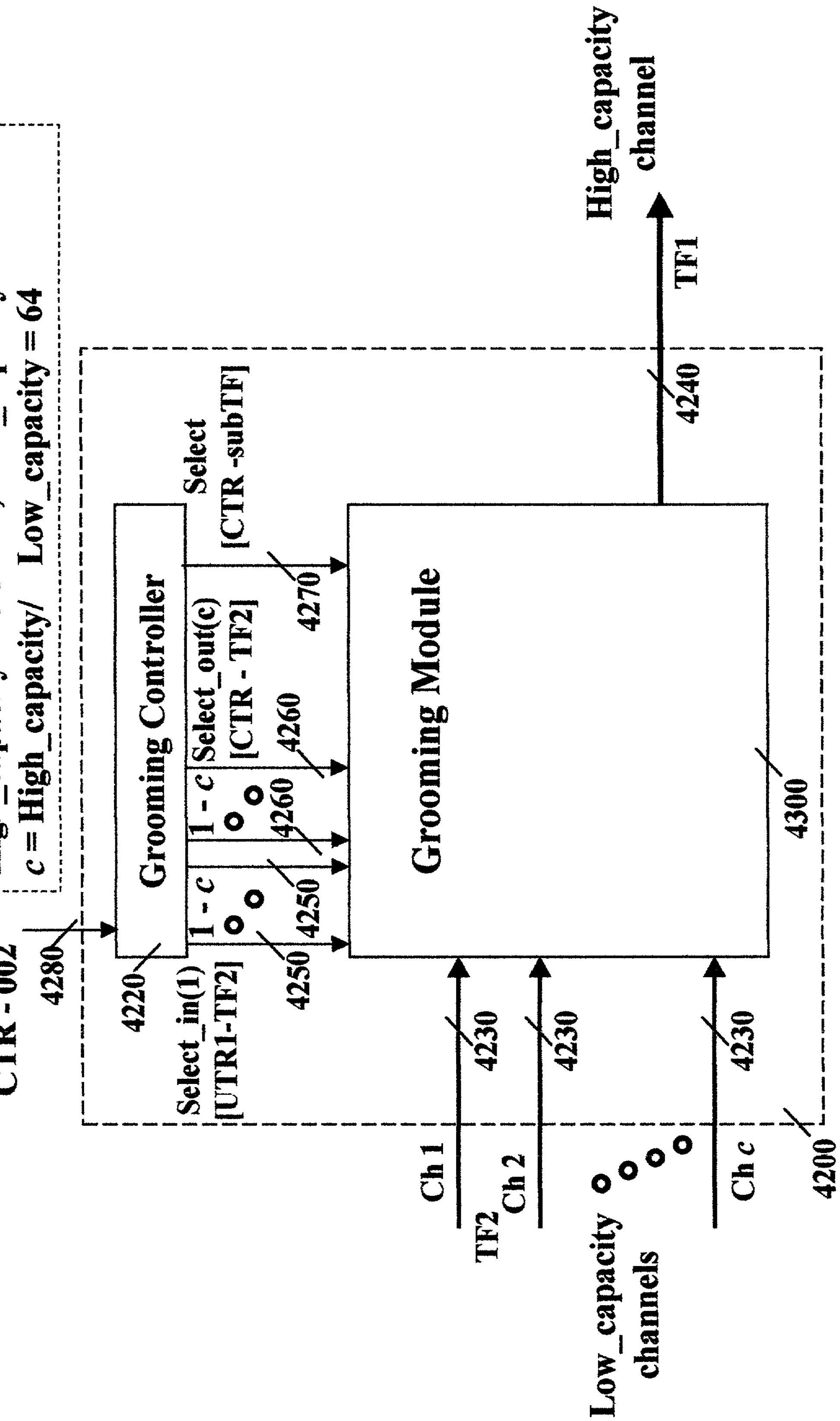


FIG. 41A

FIG. 41B

FIG. 42


High_capacity = OC-192; Low_capacity = OC-3
c = High_capacity/ Low_capacity = 64
CTR - 002
4280
Grooming Controller
4220
Select_in(1)
[UTR1-TF2]
1 - c
4250
4250
1 - c
4260
Select_out(c)
[CTR - TF2]
4260
Select
[CTR -subTF]
4270
Grooming Module
4300
4240
TF1
High_capacity
channel
4230
4230
4230
Ch 1
TF2
Ch 2
Ch c
Low_capacity
channels
4200

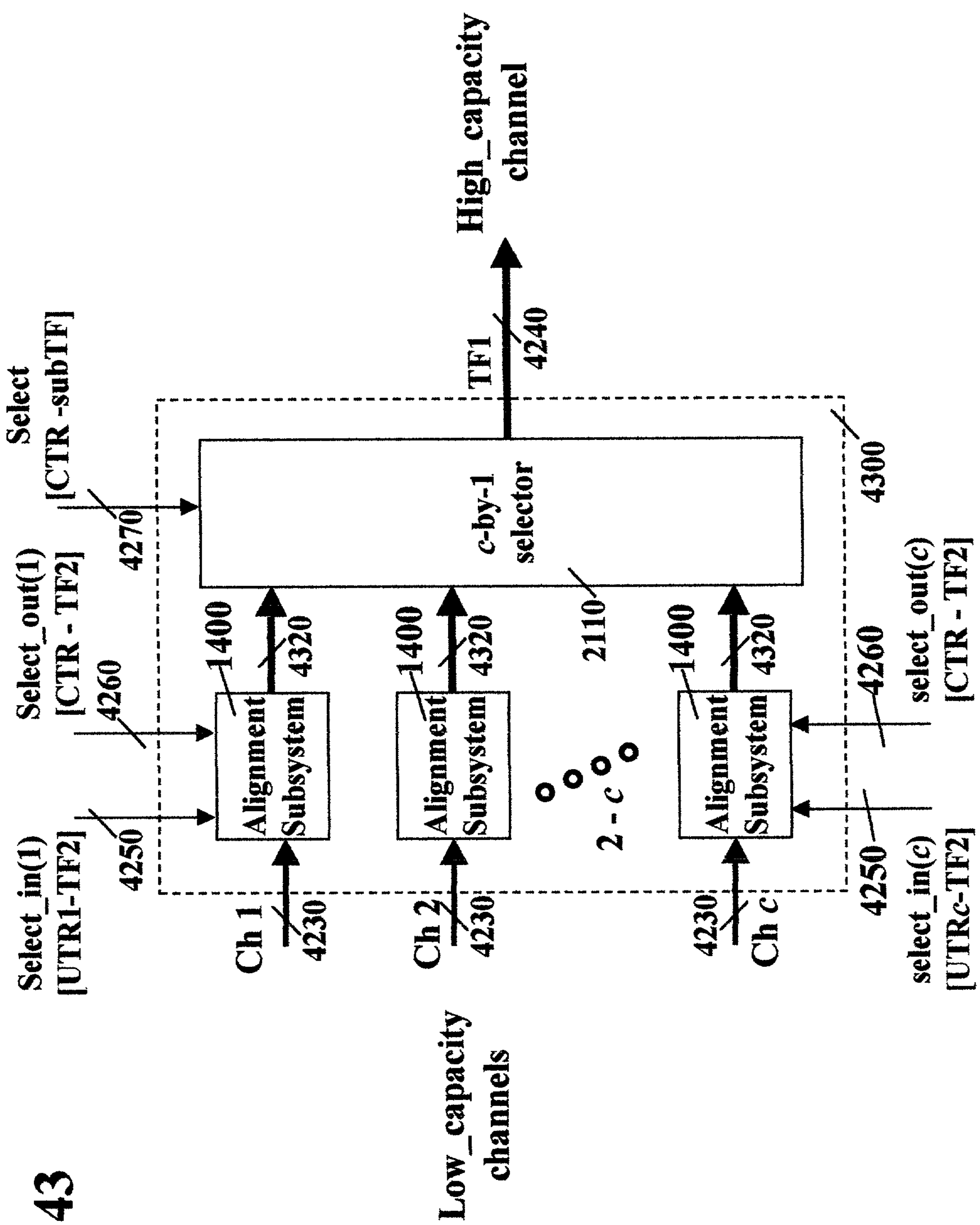

High_capacity channel
TF1
4240
Select [CTR -subTF]
4270
c-by-1 selector
2110
4300
Select_out(1) [CTR - TF2]
4260
Select_in(1) [UTR1-TF2]
4250
Alignment Subsystem
1400
4320
Ch 1
4230
Ch 2
2 - c
Ch c
select_out(c) [CTR - TF2]
select_in(c) [UTRc-TF2]
Low_capacity channels

FIG. 43

FIG. 44

- $CC1\_length \cdot TF1 = CC2\_length \cdot TF2 = CC3\_length \cdot TF2$
- $TF2 = (SC1\_length / SC2\_length) \cdot TF1 = k \cdot TF1$, where the common cycles of ***TF1*** and ***TF2*** are aligned with respect to UTC.

For $k = 2$ and $c = 4$ (e.g., High_capacity=OC-192, Low_capacity=OC-48):

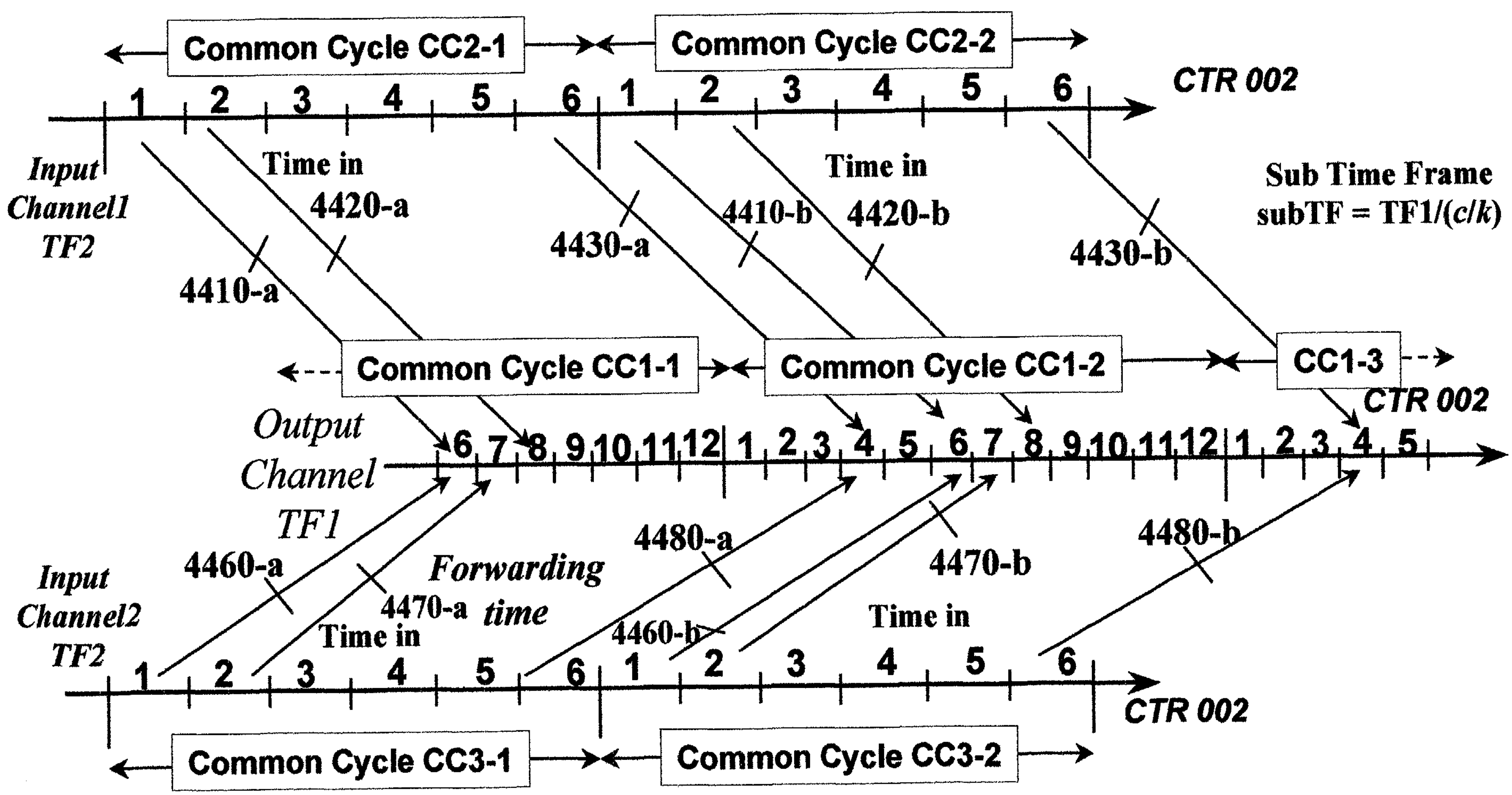
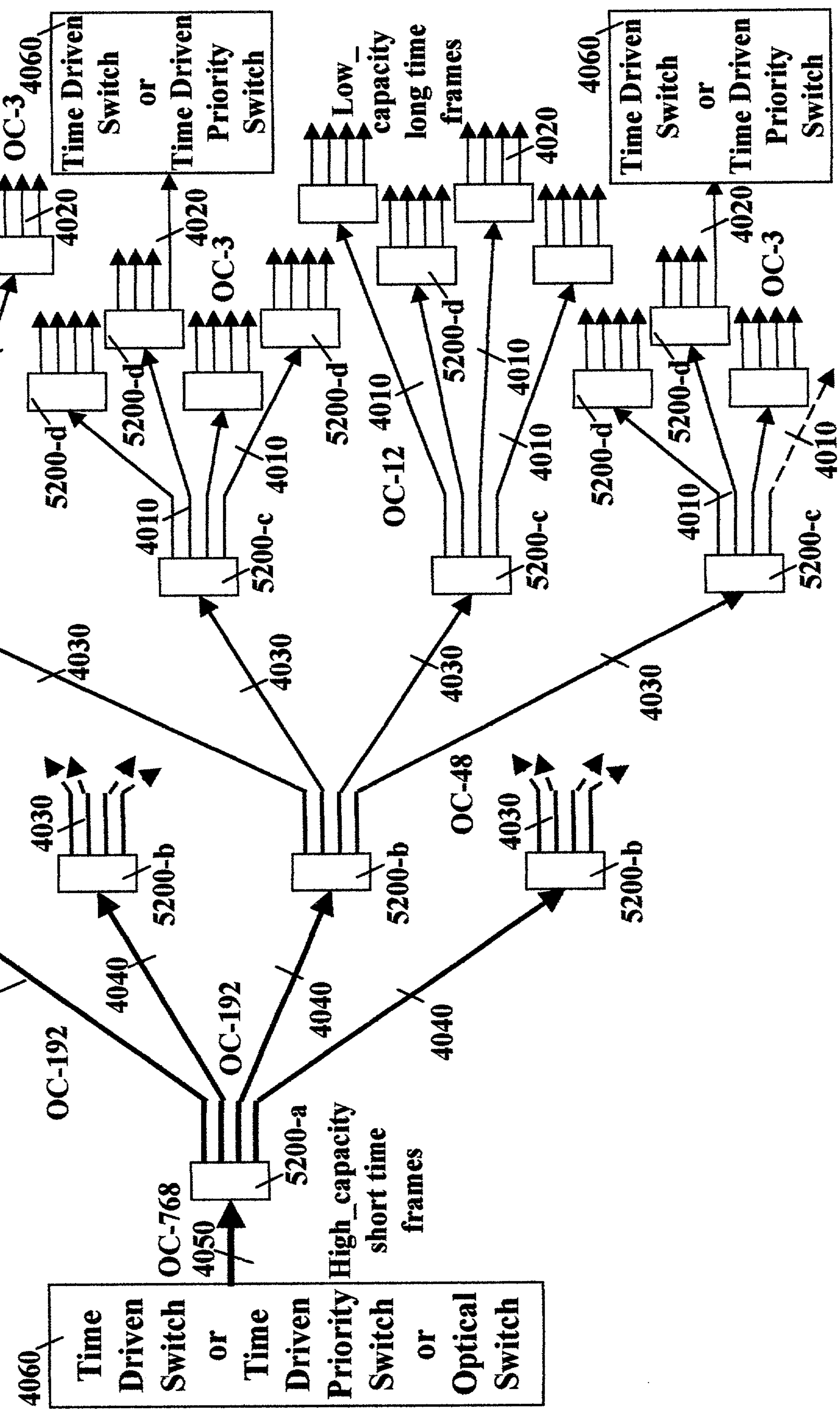


FIG. 45


4060
Time Driven Switch or Time Driven Priority Switch or Optical Switch
OC-768
4050
High_capacity short time frames
5200-a
OC-192
4040
5200-b
4030
OC-48
5200-c
OC-12
4010
5200-d
4020
OC-3
Low_capacity long time frames
Time Driven Switch or Time Driven Priority Switch

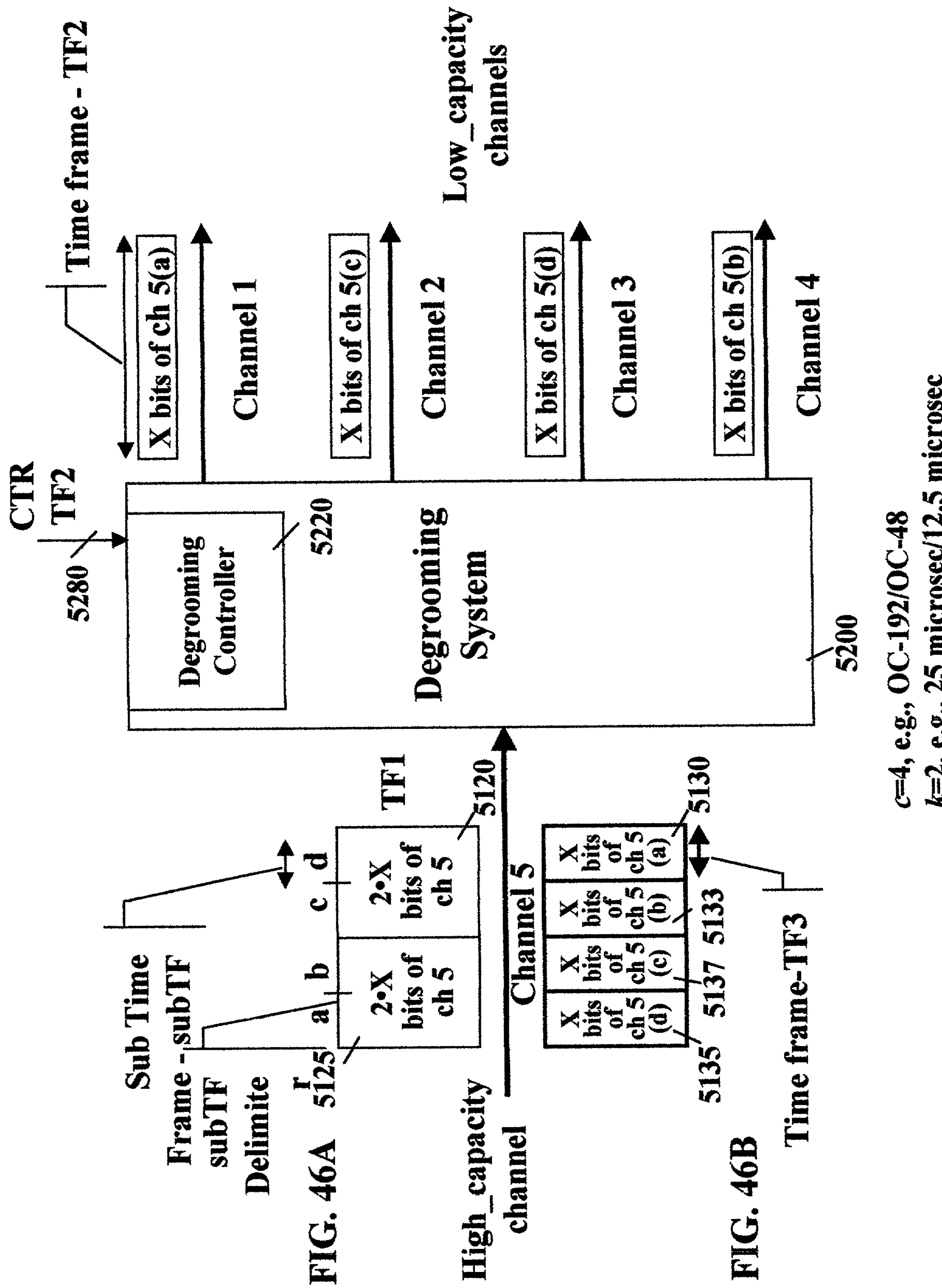


FIG. 46A

FIG. 46B

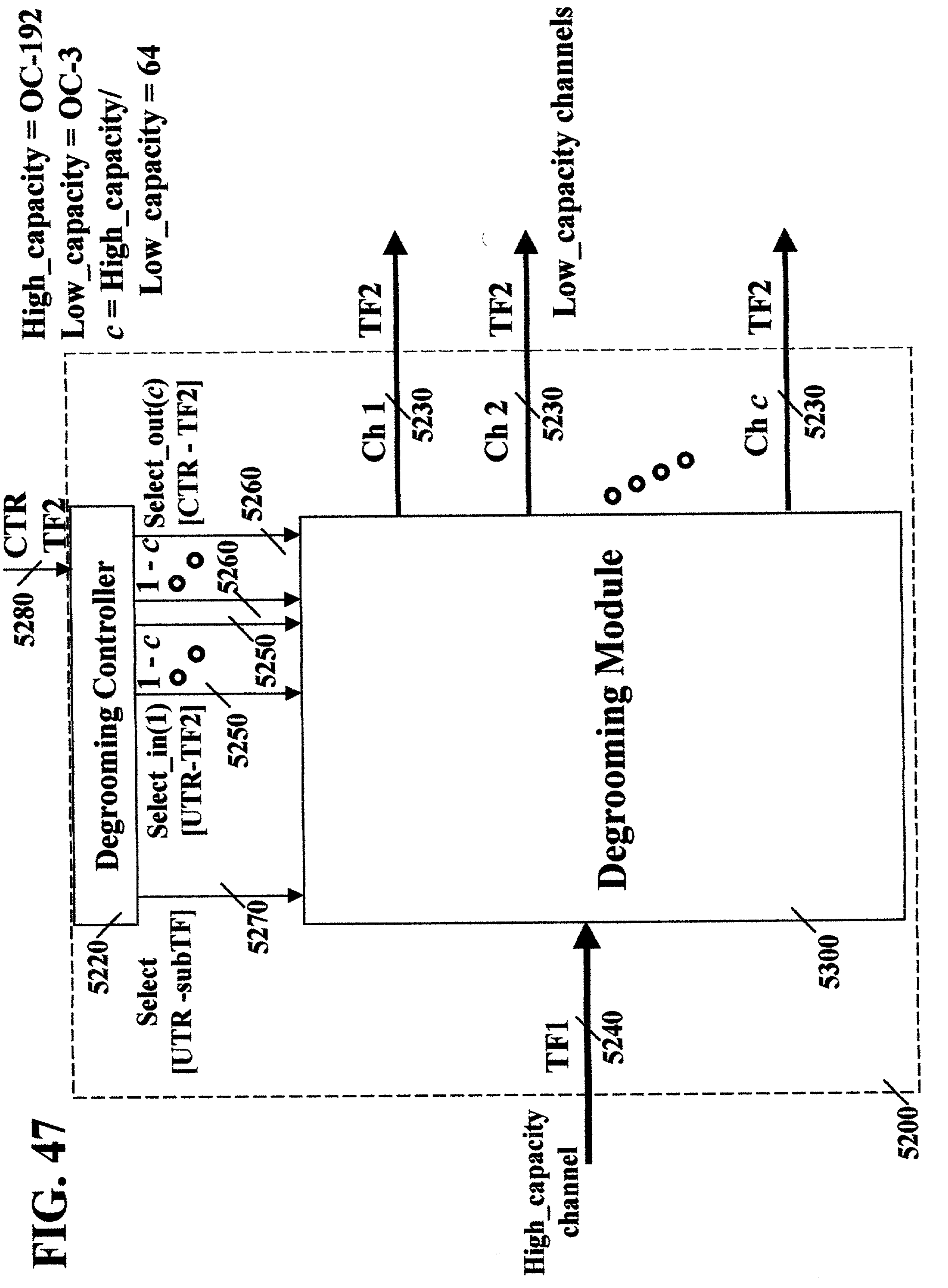

High_capacity = OC-192
Low_capacity = OC-3
c = High_capacity/
Low_capacity = 64
CTR
TF2
5280
Degrooming Controller
5220
Select
[UTR -subTF]
5270
Select_in(1)
[UTR-TF2]
5250
1 - c
5250
1 - c
5260
Select_out(c)
[CTR - TF2]
5260
Degrooming Module
5300
Ch 1
5230
TF2
Ch 2
5230
TF2
Ch c
5230
TF2
Low_capacity channels
High_capacity channel
TF1
5240
5200

FIG. 47

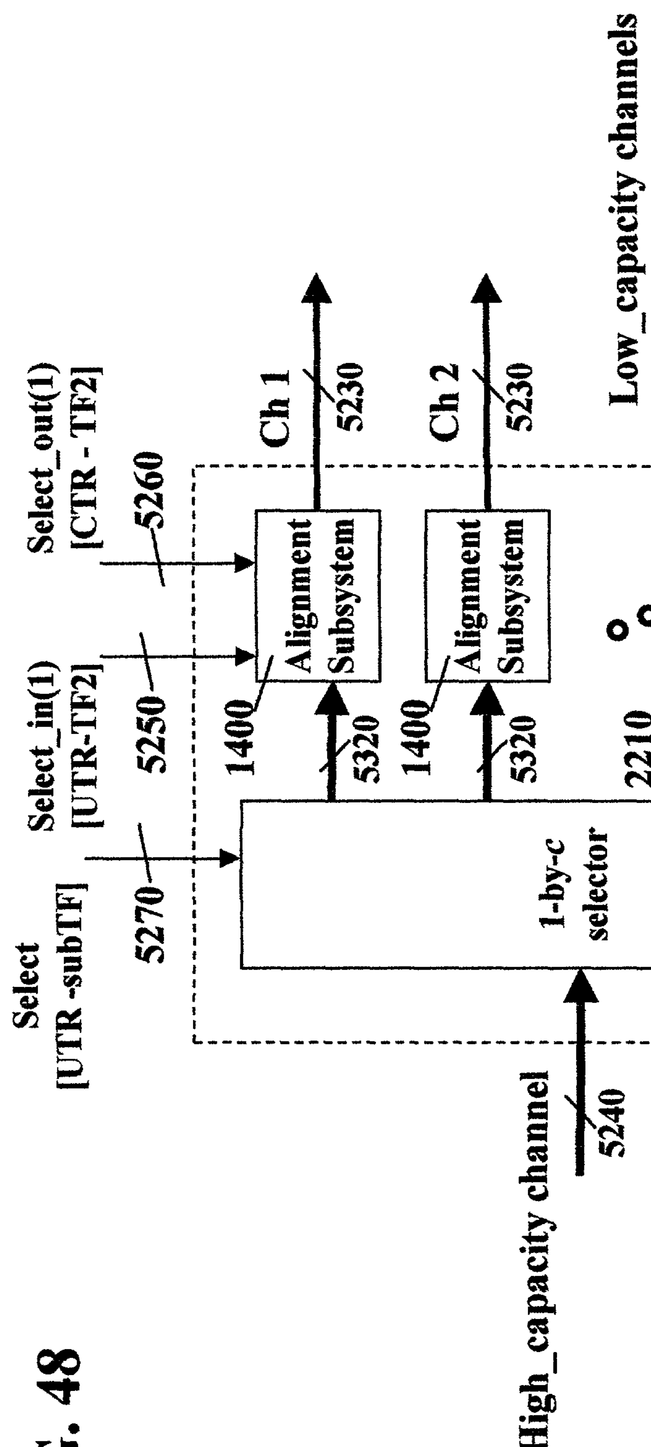
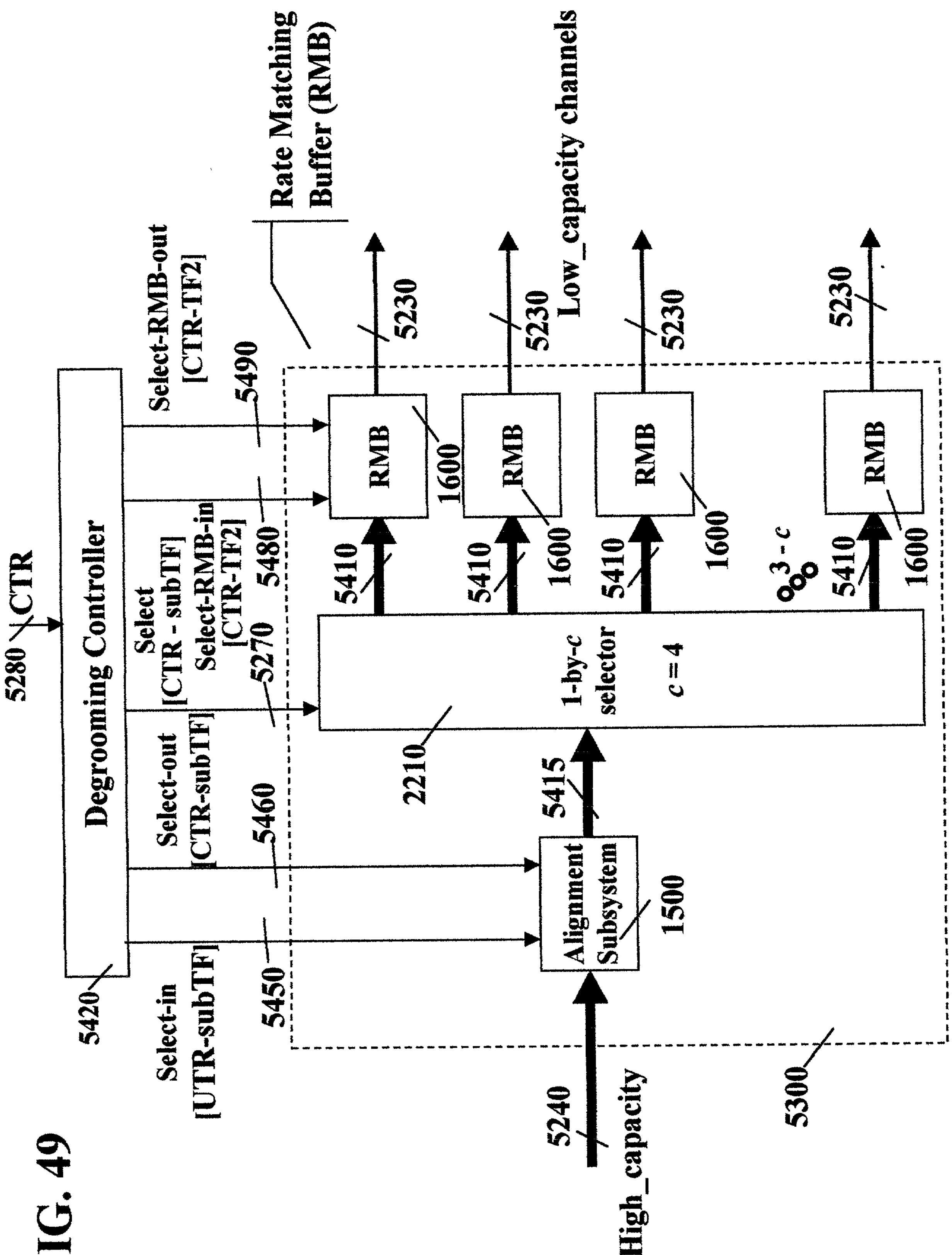

Low_capacity channels
Ch 1
Ch 2
Ch c
5230
Select_out(1)
[CTR - TF2]
Select_in(1)
[UTR-TF2]
Select
[UTR -subTF]
5260
5250
5270
Alignment Subsystem
1400
5320
2210
2 - c
1-by-c selector
5300
Select_out(c)
[CTR - TF2]
Select_in(c)
[UTR-TF2]
High_capacity channel
5240

FIG. 48

FIG. 49


Degrooming Controller
5280
CTR
5420
Select-in [UTR-subTF]
5450
Select-out [CTR-subTF]
5460
Select [CTR - subTF]
5270
Select-RMB-in [CTR-TF2]
5480
Select-RMB-out [CTR-TF2]
5490
Rate Matching Buffer (RMB)
Low_capacity channels
5230
RMB
1600
5410
1-by-c selector
c = 4
3 - c
2210
5415
Alignment Subsystem
1500
5240
High_capacity
5300

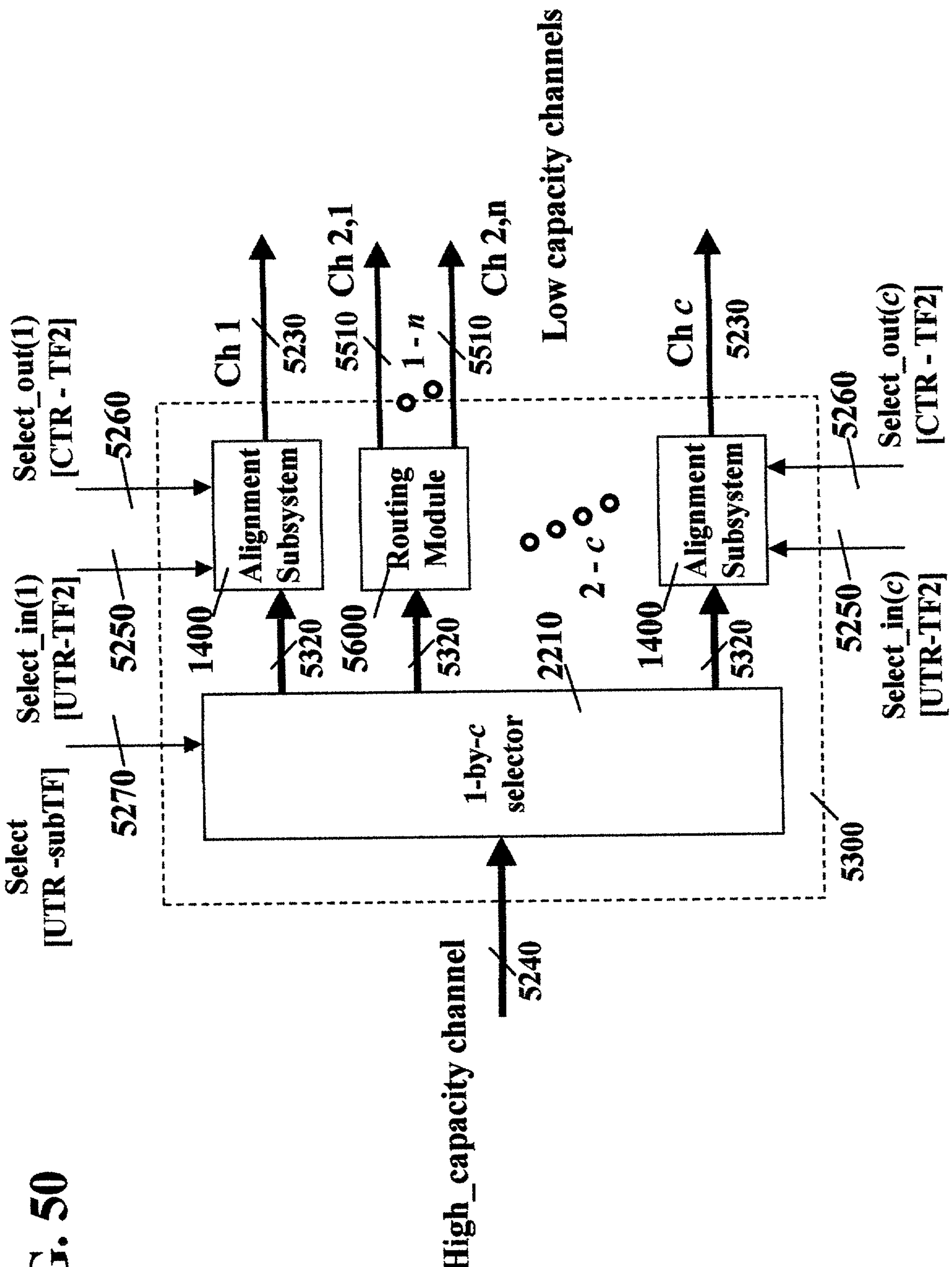

High_capacity channel
5240
Select
[UTR -subTF]
5270
1-by-c
selector
2210
5300
Select_in(1)
[UTR-TF2]
5250
Select_out(1)
[CTR - TF2]
5260
1400
Alignment
Subsystem
5320
5600
Routing
Module
2 - c
Ch 1
5230
5510 Ch 2,1
1 - n
5510
Ch 2,n
Low capacity channels
Ch c
5230
5260
Select_out(c)
[CTR - TF2]
5250
Select_in(c)
[UTR-TF2]

FIG. 50

FIG. 51

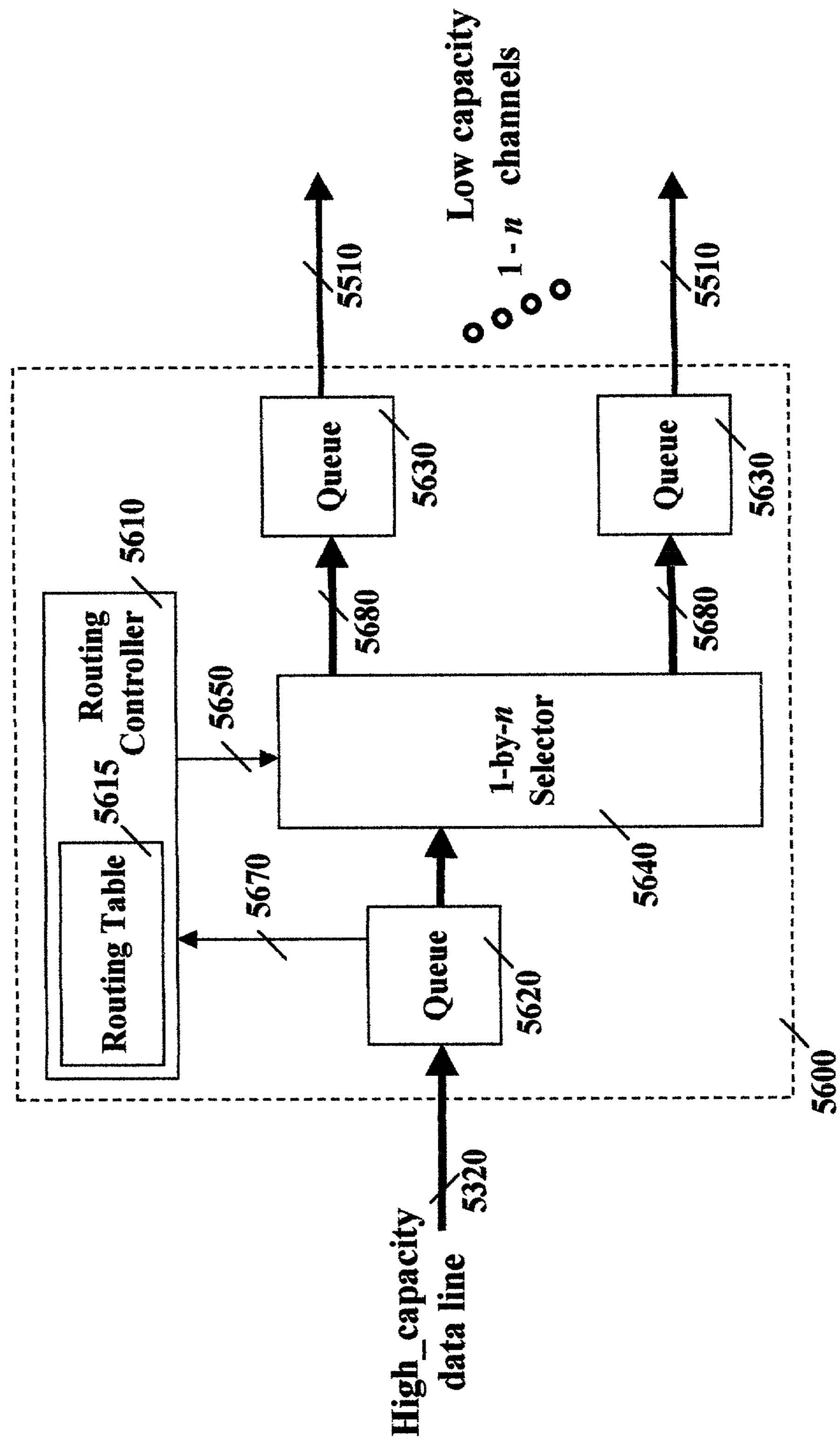
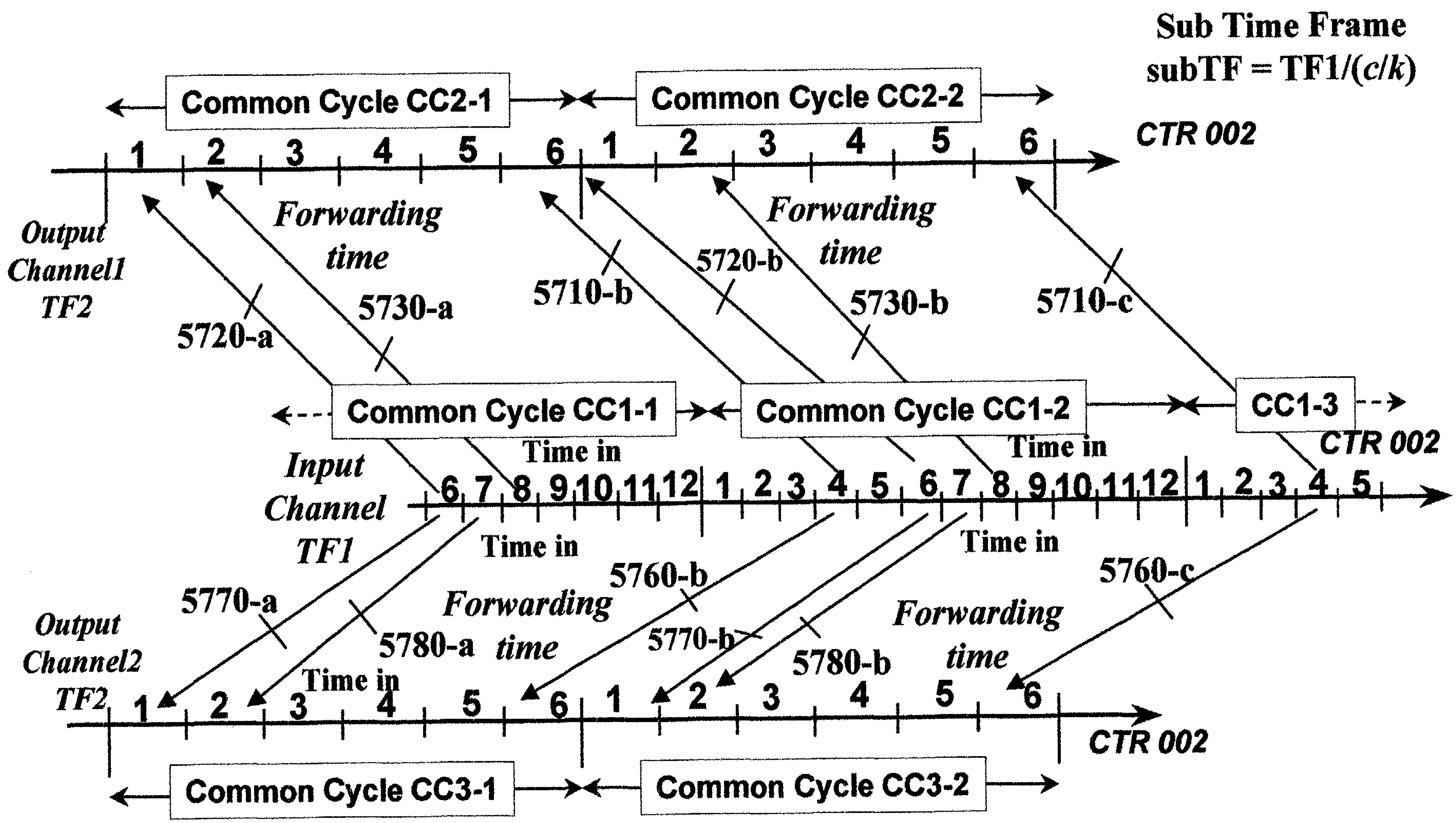

High_capacity data line
5320
5600
Queue
5620
Routing Table
5615
Routing Controller
5610
5670
5650
1-by-n Selector
5640
5680
5680
Queue
5630
Queue
5630
5510
5510
1 - n
Low capacity channels

FIG. 52

- ***CC1_length·TF1 = CC2_length·TF2 = CC3_length·TF2***
- ***TF2 = (SC1_length / SC2_length) · TF1 = k · TF1***, where the common cycles of ***TF1*** and ***TF2*** are aligned with respect to UTC.

For $k = 2$ and $c = 4$ (e.g., High_capacity=OC-192, Low_capacity=OC-48):



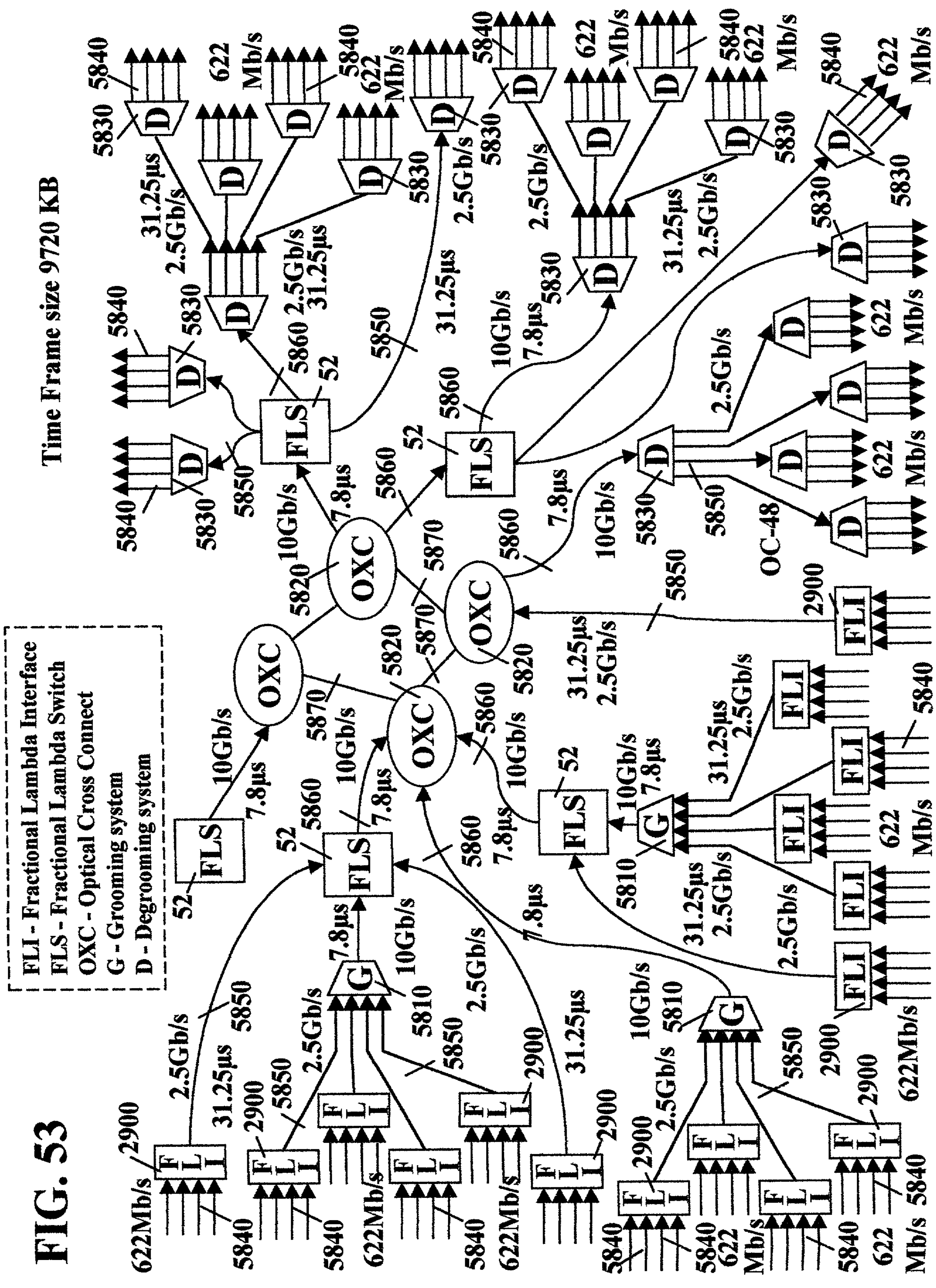

Time Frame size 9720 KB
FLI - Fractional Lambda Interface
FLS - Fractional Lambda Switch
OXC - Optical Cross Connect
G - Grooming system
D - Degrooming system
FLS
OXC
FLI
G
D
10Gb/s
7.8μs
2.5Gb/s
31.25μs
622Mb/s
OC-48
52
2900
5810
5820
5830
5840
5850
5860
5870

FIG. 53

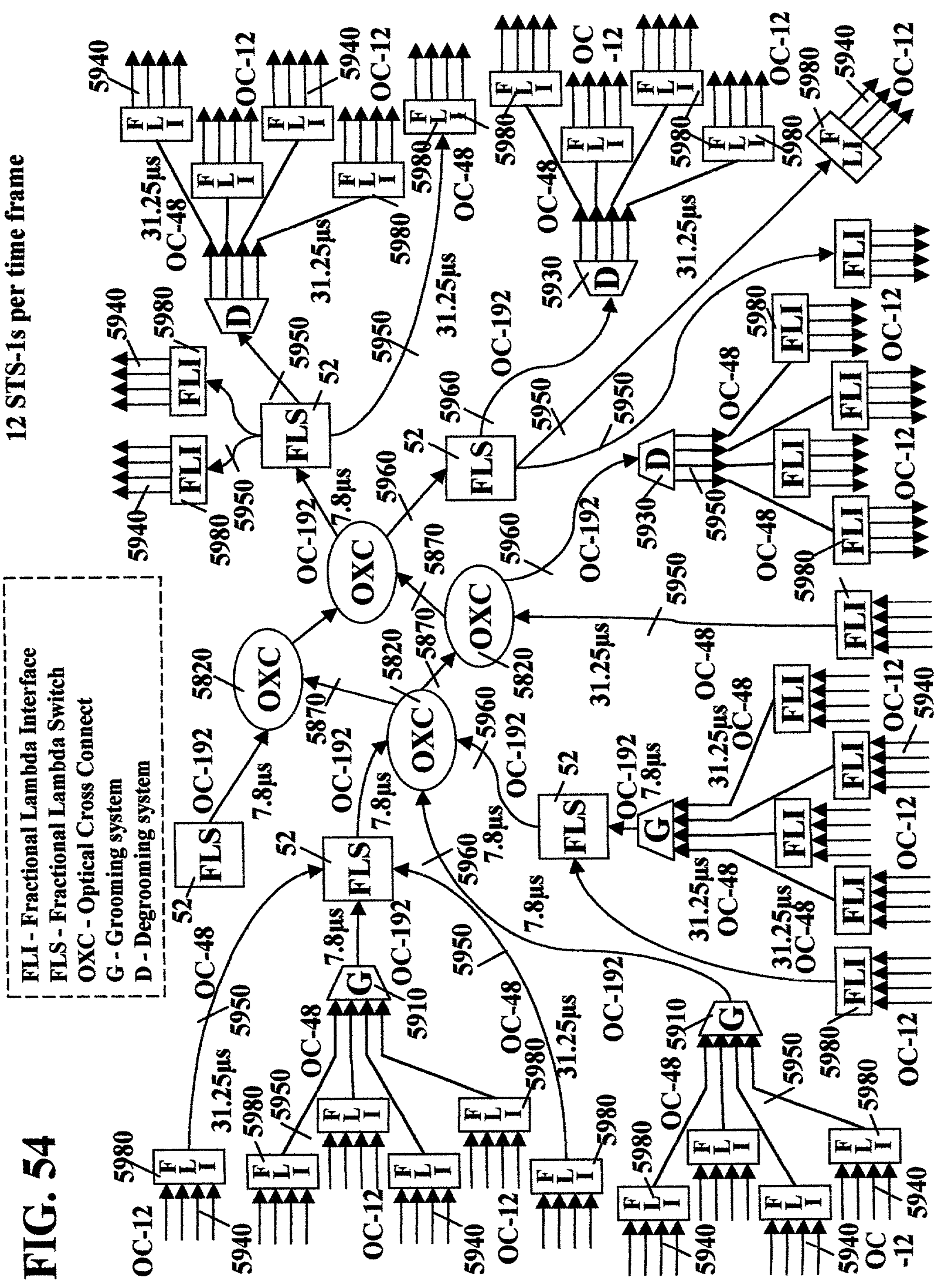
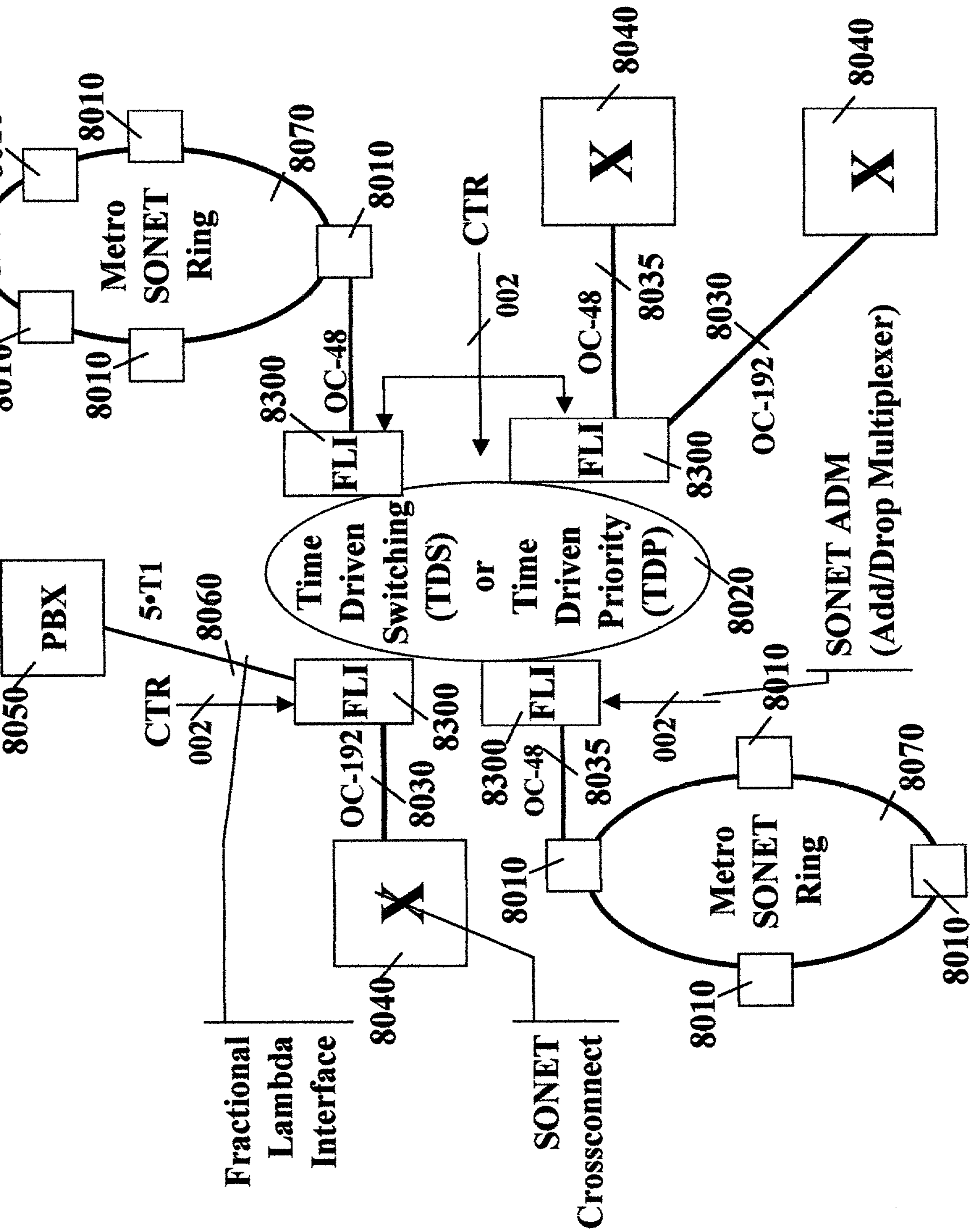

12 STS-1s per time frame
FLI - Fractional Lambda Interface
FLS - Fractional Lambda Switch
OXC - Optical Cross Connect
G - Grooming system
D - Degrooming system
FLI
FLS
OXC
G
D
OC-12
OC-48
OC-192
7.8μs
31.25μs
52
5820
5870
5910
5930
5940
5950
5960
5980

FIG. 54

FIG. 55


Metro SONET Ring
8070
8010
OC-48
8300
FLI
CTR
002
8040
X
8035
8030
OC-192
Time Driven Switching (TDS) or Time Driven Priority (TDP)
8020
SONET ADM (Add/Drop Multiplexer)
PBX
8050
5•T1
8060
Fractional Lambda Interface
SONET Crossconnect

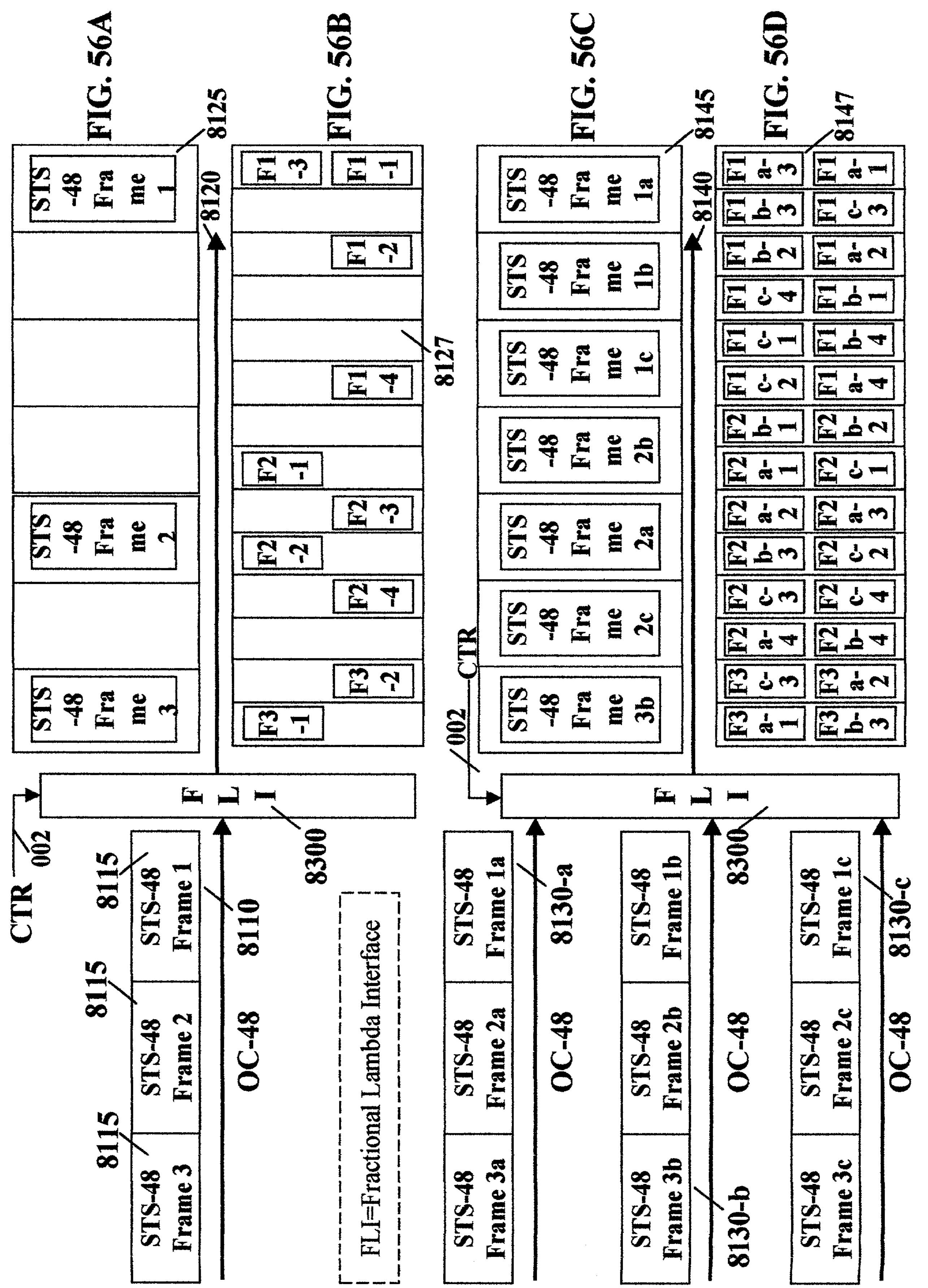


FIG. 56A

FIG. 56B

FIG. 56C

FIG. 56D

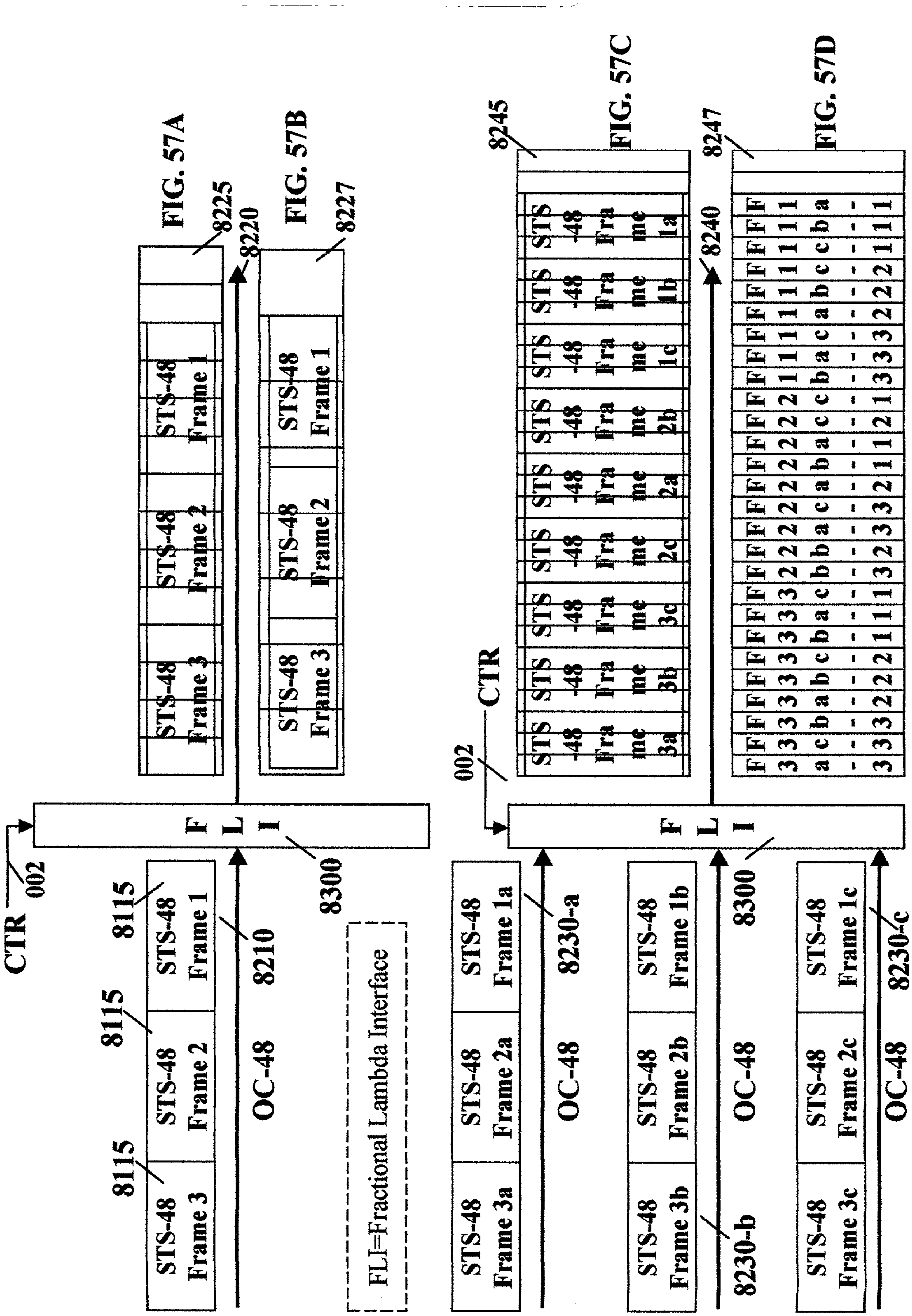


FIG. 57A

FIG. 57B

FIG. 57C

FIG. 57D

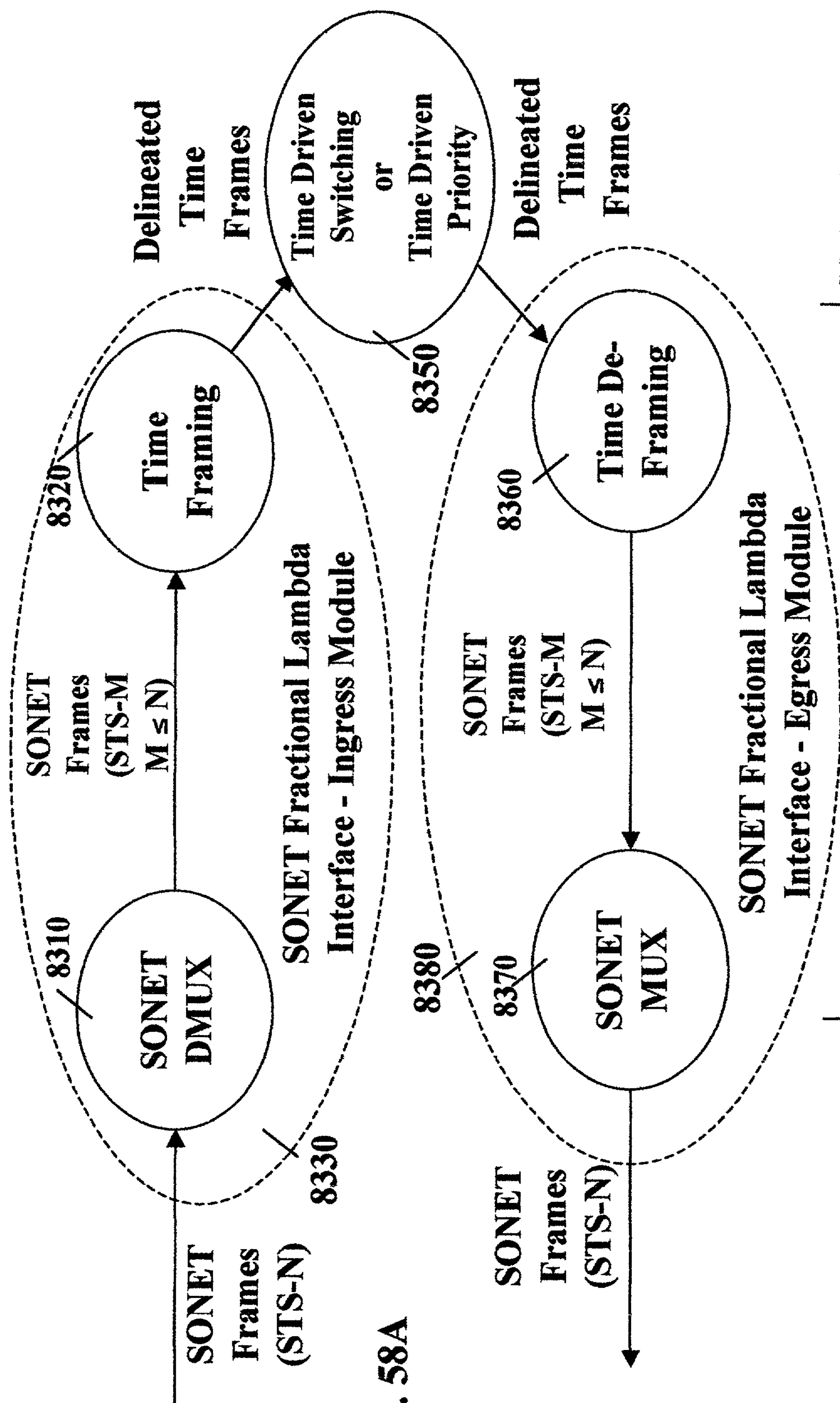


FIG. 58A

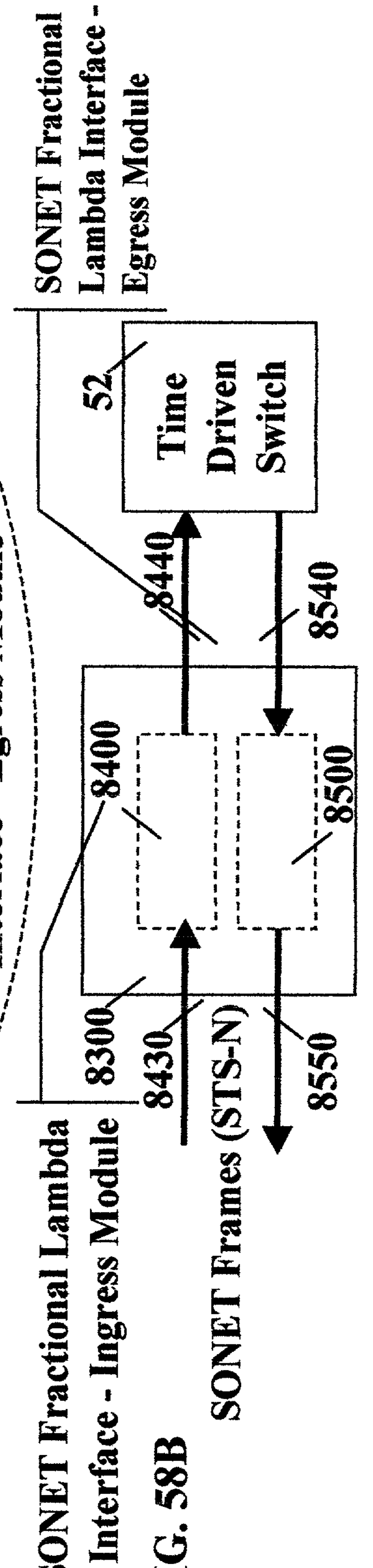
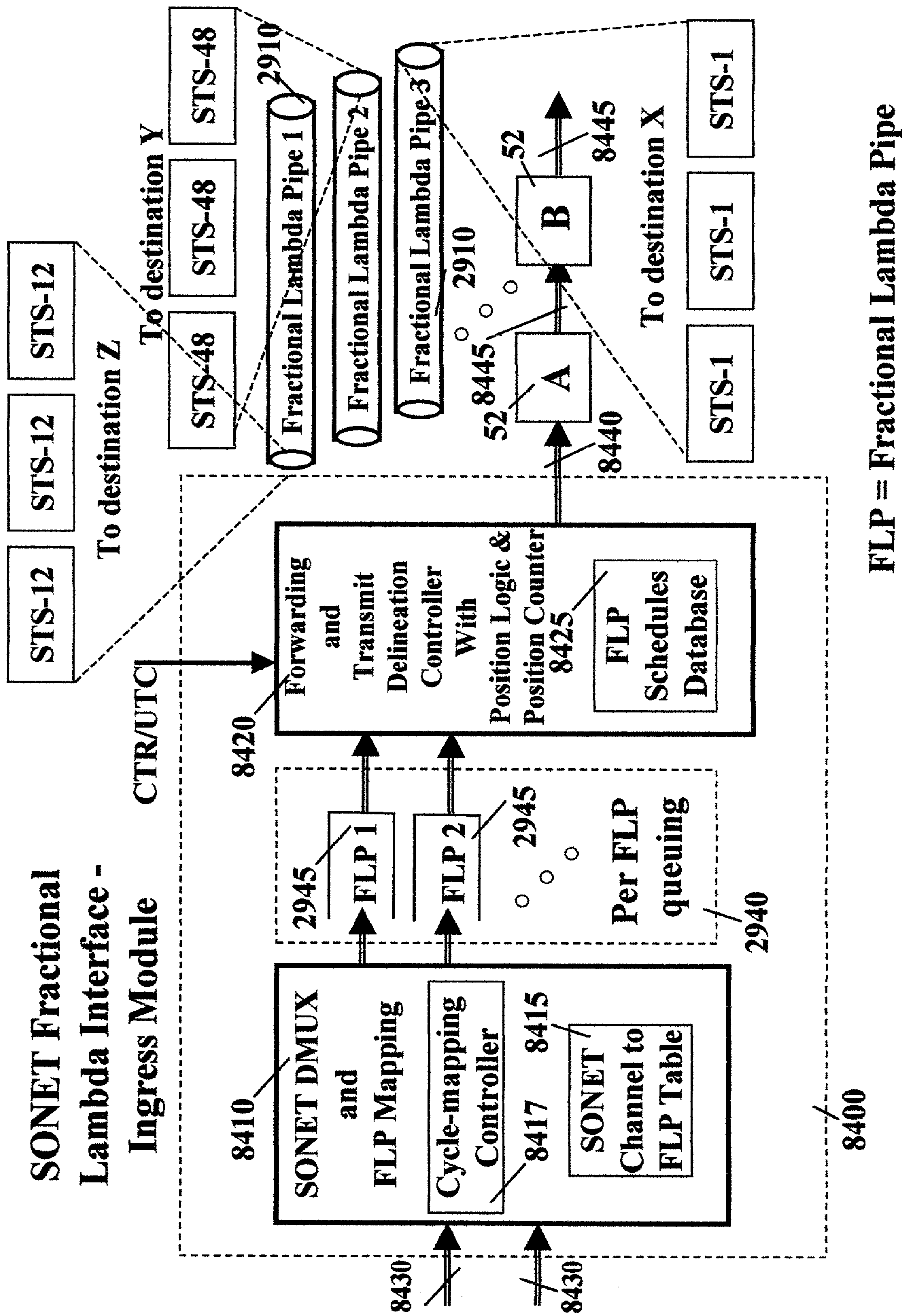


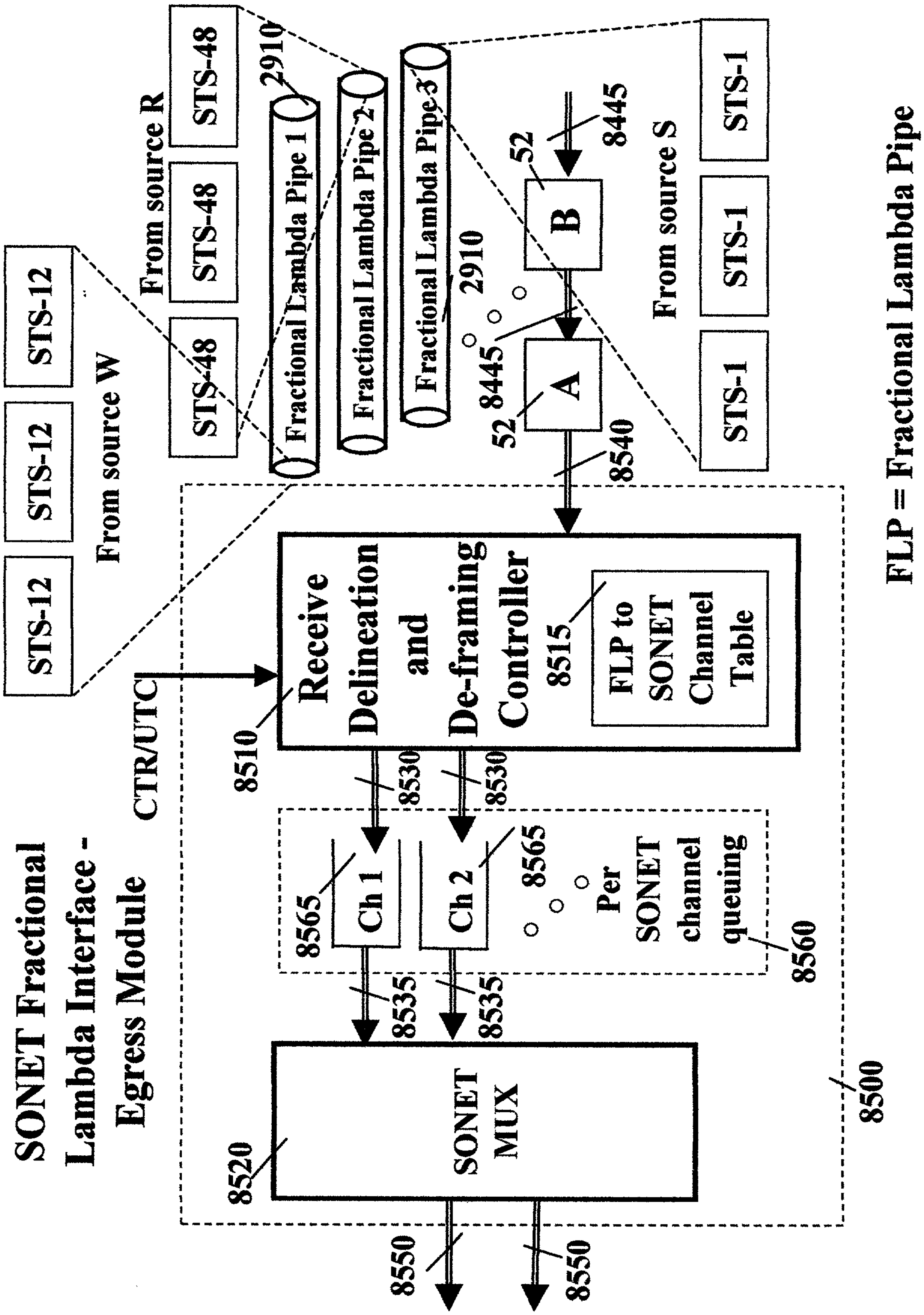
FIG. 58B

FIG. 59



FLP = Fractional Lambda Pipe

FIG. 60


SONET Fractional Lambda Interface - Egress Module
From source W
STS-12
STS-12
STS-12
From source R
STS-48
STS-48
STS-48
From source S
STS-1
STS-1
STS-1
Fractional Lambda Pipe 1
Fractional Lambda Pipe 2
Fractional Lambda Pipe 3
2910
2910
A
B
52
52
8445
8445
8540
CTR/UTC
Receive Delineation and De-framing Controller
8510
FLP to SONET Channel Table
8515
8530
8530
Ch 1
Ch 2
8565
8565
Per SONET channel queuing
8560
8535
8535
SONET MUX
8520
8500
8550
8550
FLP = Fractional Lambda Pipe

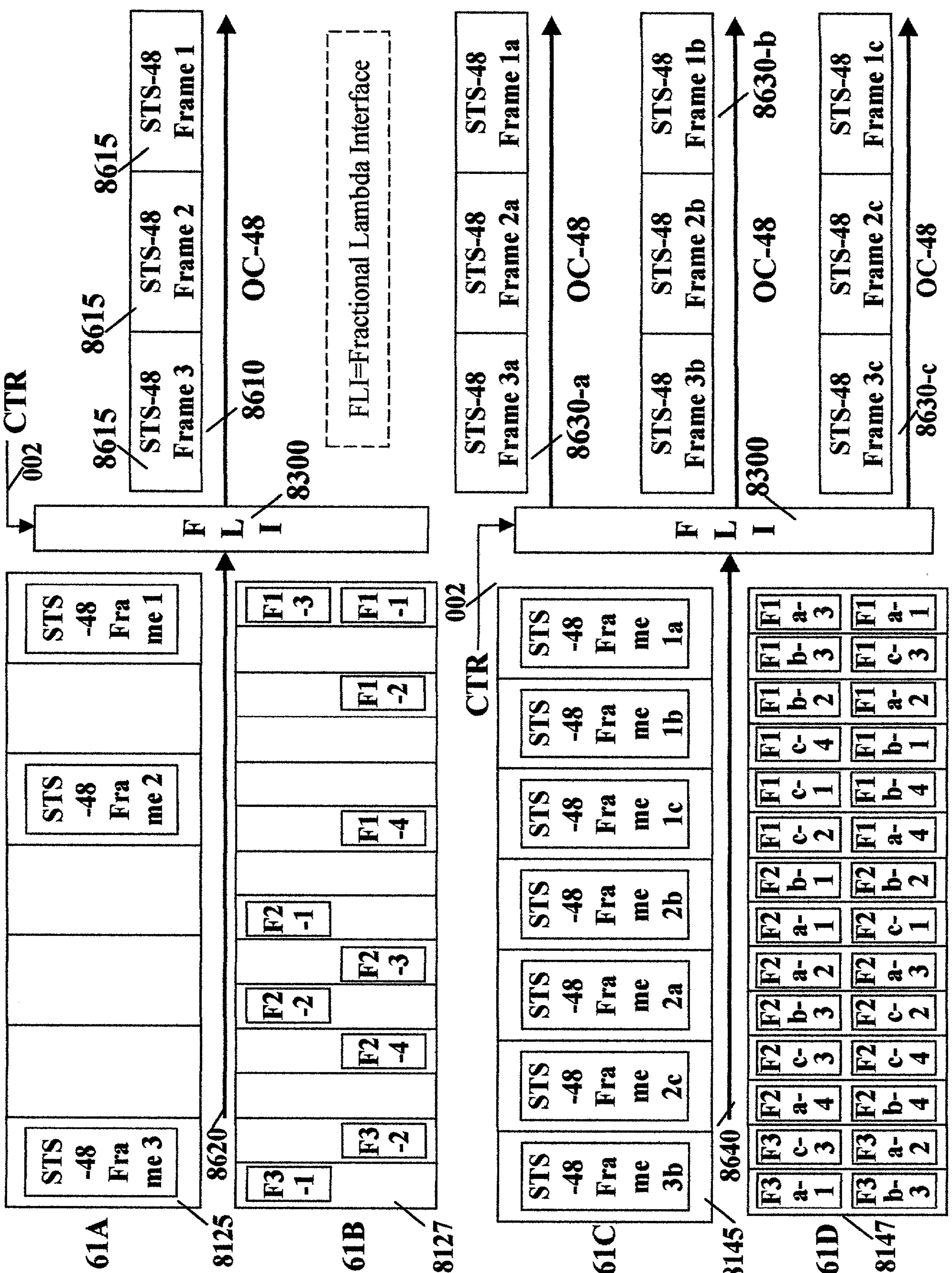


FIG. 61A

FIG. 61B

FIG. 61C

FIG. 61D

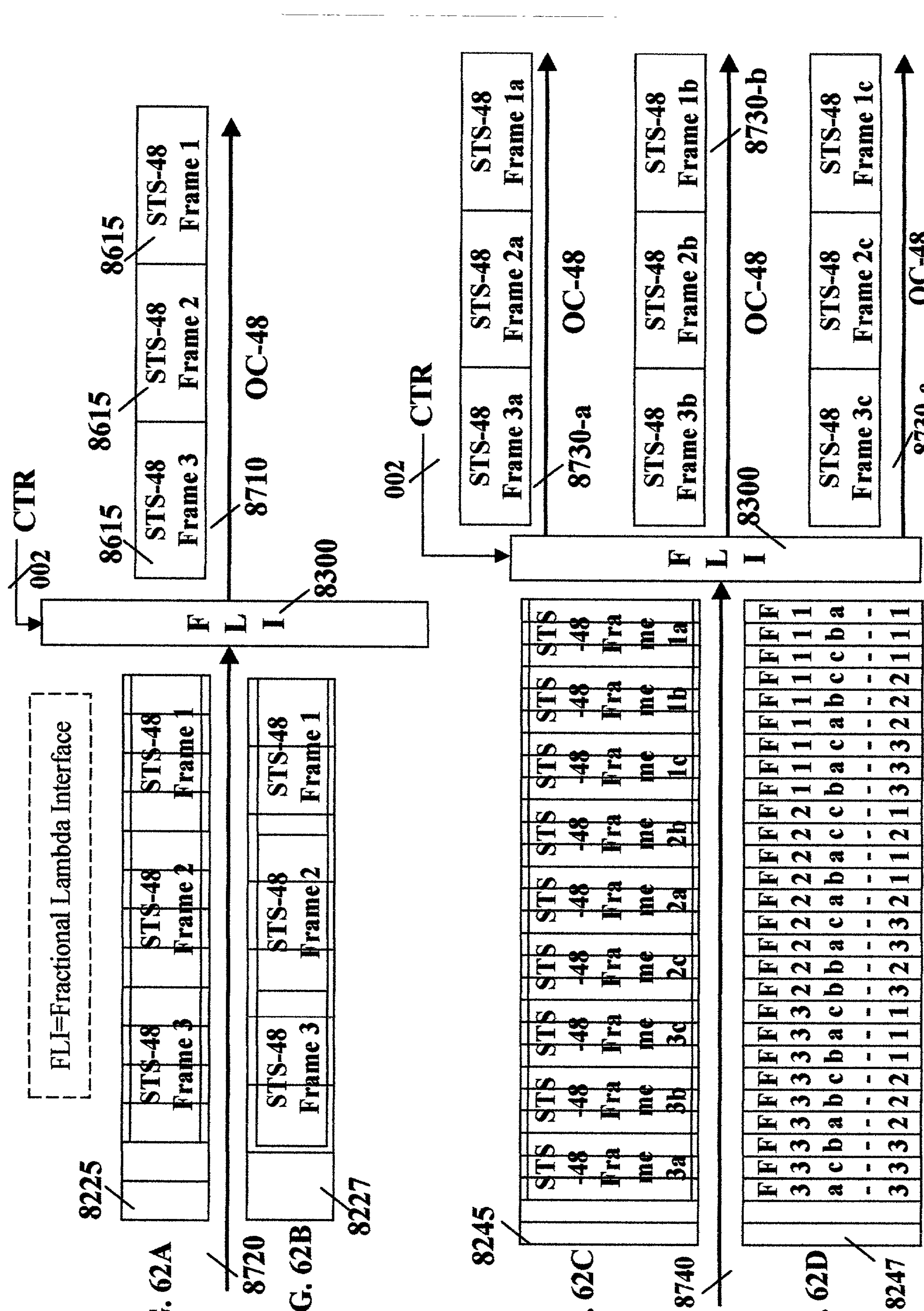


FIG. 62A

FIG. 62B

FIG. 62C

FIG. 62D

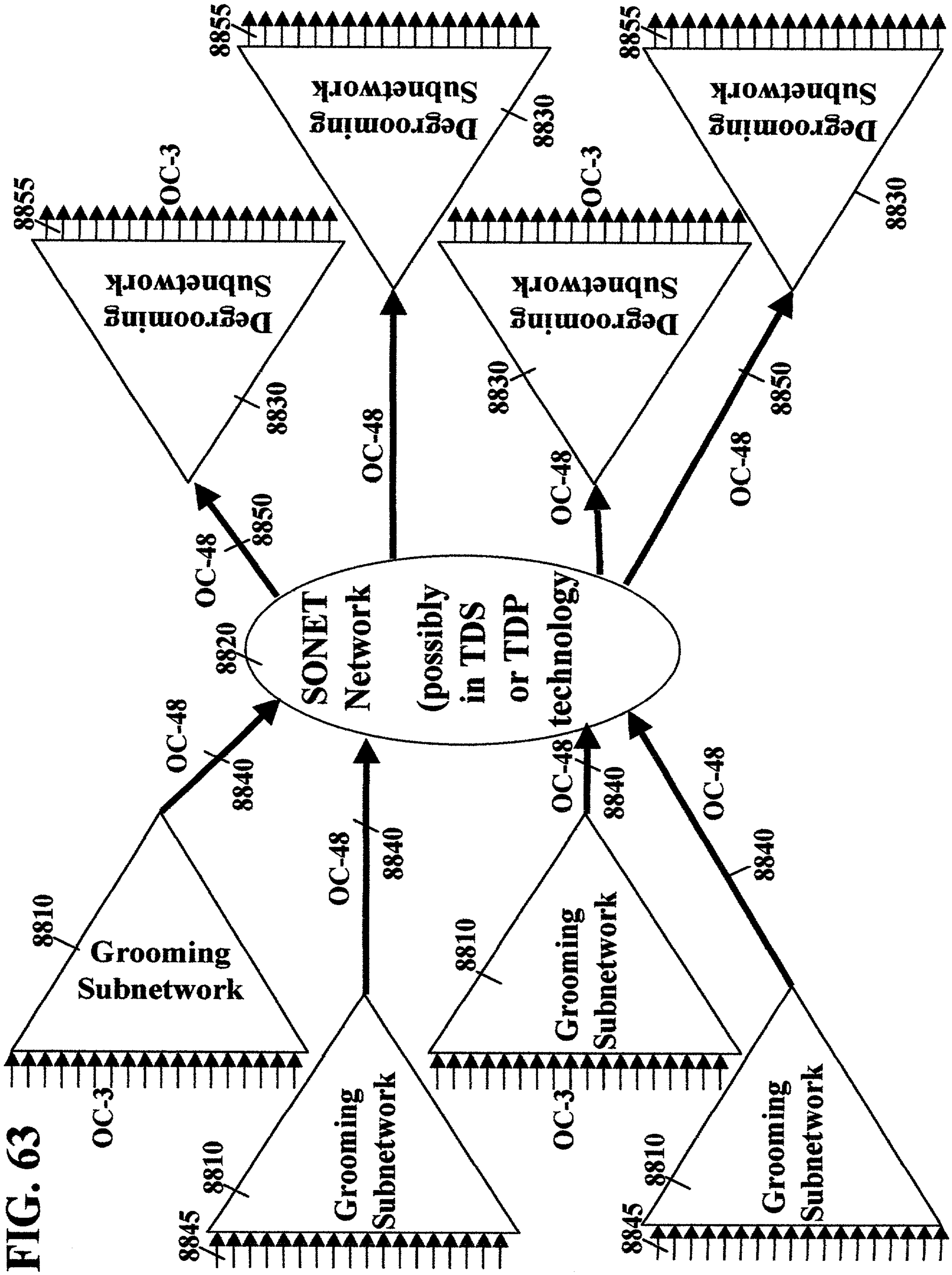
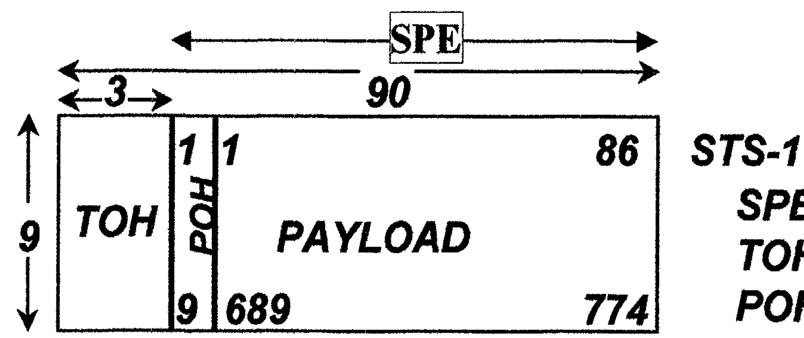

Grooming Subnetwork
8810
8845
OC-3
OC-48
8840
SONET Network (possibly in TDS or TDP technology)
8820
8850
Degrooming Subnetwork
8830
8855

FIG. 63

- SONET - synchronous optical network
- Multiplexing method: byte interleaving
- Signal hierarchy: OC-N (STS-N)
  – STS-N rate: N*51.84 Mb/s
  – Frame format: 9 rows by 90*N columns
    - capacity: N*810 bytes in 125 microsecond.
    - overhead: N*27 bytes
    - payload: N*783 bytes

FIG. 64A



SPE - Synchronous Payload Environment
TOH - Transport Overhead
POH - Path Overhead

FIG. 64B

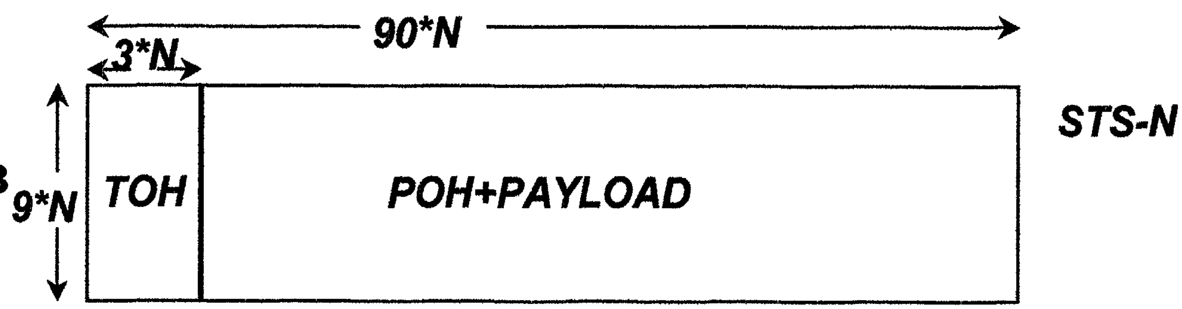
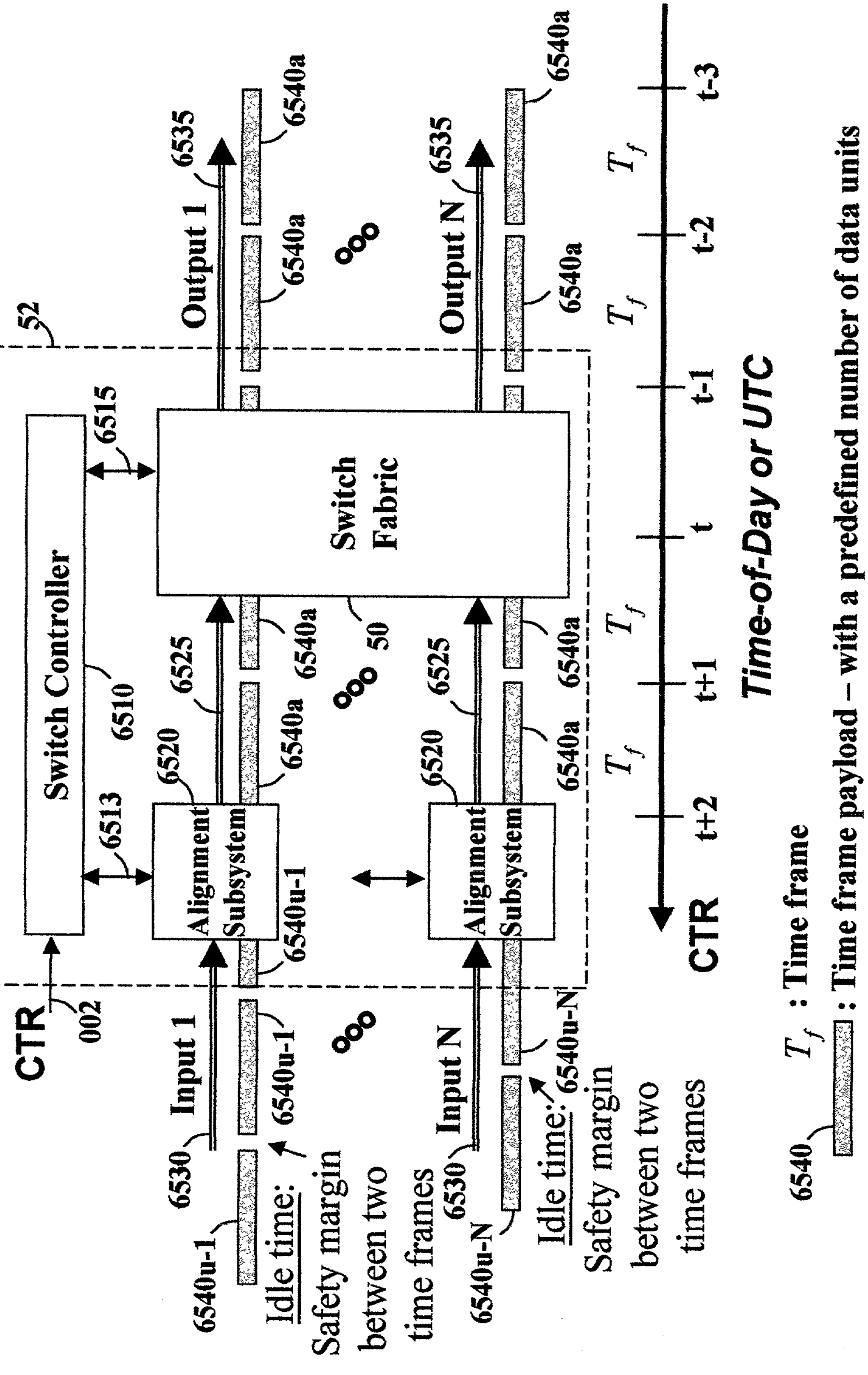


FIG. 65


CTR
002
52
Switch Controller
6510
6513
6515
Alignment Subsystem
6520
Switch Fabric
50
6525
6530
6535
Input 1
Input N
Output 1
Output N
6540u-1
6540u-N
6540a
Idle time: Safety margin between two time frames
CTR
t+2
t+1
t
t-1
t-2
t-3
T_f
Time-of-Day or UTC
T_f : Time frame
6540
: Time frame payload – with a predefined number of data units